

Xiya Zhou

xyz137@stanford.edu | (352) 745-5346 | linkedin.com/in/xz137

Education

Stanford University - Stanford, CA

Expected Graduation: December 2027

Incoming Master of Science in Electrical Engineering

University of Florida (UF) - Gainesville, FL

Aug 2022 - May 2026

Bachelor of Science in Electrical Engineering

GPA: 4.0/4.0

- **Relevant Coursework:** Analog IC Design 1&2, Fundamentals of Data Converters, VLSI 1&2, High Speed Links
- **Technical Skills:** Cadence Virtuoso (ADE Explorer, Caliber DRC/LVS/PEX), MATLAB, KiCAD

Internship Experience

Texas Instruments

May 2025 - August 2025, July 2026 – September 2026

Analog IC Design Intern – Current and Magnetic Sensing Team

Tucson, AZ

- Executed the design refresh of a current monitor IC, migrating the legacy BJT-only design into a modern **Bi-CMOS process** while maintaining performance and reducing die cost
- Verified design robustness across PVT variations using **Monte Carlo simulations**, ensuring reliable operation over supply and common-mode voltages up to 60V
- Evaluated five **bandgap reference generator** topologies, analyzing trade-offs in startup behavior, PSRR, and die area
- Reduced overall die cost by **over 60%**, generating over six figures in projected annual savings for product line

Publications

- W. Han, **X. Zhou**, J. Wan, Y. Zhao, C. Cheng, and A. Khalifa, “A Wireless Multimodal Microchip for Integrated Neural Stimulation, Recording, and Dopamine Monitoring,” accepted for presentation at the IEEE Midwest Symposium on Circuits and Systems (MWSCAS), Cincinnati, Ohio, Aug. 2026.
- R. Wang, O. Sen, **X. Zhou**, W. Han, A. Katikhaneni, A. Khalifa, and B. Chatterjee, “Analog-To-Time-Conversion Assisted Low-Power Inferencing for Epileptic Seizures,” presented at the IEEE Midwest Symp. on Circuits and Systems (MWSCAS), Lansing, Michigan, Aug. 2025

Research Experience

UF Neural Interface Technology Lab (Professor Adam Khalifa)

December 2024 – December 2025

- Collaborated with PhD mentor to tape-out an implantable biomedical IC in TSMC’s **65nm** technology node which incorporates neural stimulation, recording, and dopamine sensing on a single platform
- Designed and created layout for 8-bit **Analog to Time Converter (Single-Slope ADC)** and wireless telemetry blocks, employing **switched-capacitor, dynamic comparator, and sequential logic circuits** to encode neural recording output into PWM waveforms, and wirelessly transmit them using Load Shift Keying to devices outside the brain
- Achieved energy consumption per 8-bit conversion-step (Walden FOM) of 11fJ for the ATC in post-PEX simulation, **2.7x lower** than SAR ADCs with the same resolution

Selected Mixed-Signal IC Design Projects

- Designed a pseudo-differential **ring-amplifier** ADC front-end in 180nm technology node with resistor-based dead-zone embedding, achieving **62.8 dB SINAD at 100 MS/s** for near-Nyquist inputs while consuming **less than 3mW** of power
- Created transistor-level implementation of a **12-bit 2nd-order discrete-time delta-sigma ADC** using switched-capacitor integrators, achieving **ENOB of 11.56** over 50 kHz bandwidth using an Oversampling Ratio (OSR) of 64

Activities

UF Department of Electrical and Computer Engineering

August 2023 – December 2025

Teaching Assistant (Circuits 1, Digital Logic, Microprocessors, Signals & Systems, Electronic Circuits 2)

- Held office hours and graded assignments for **450+ students** over 5 semesters for 5 different EE classes, providing individualized support and feedback to strengthen understanding of foundational EE concepts