

CADEN DAVIS

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EDUCATION

Stanford University

Palo Alto, CA

Master of Science in Electrical Engineering (MSEE)

September 2025 – Graduating June 2027

Specialization in Signal Processing (DSP) and Wireless Communications | Breadth Areas in ML and VLSI

University of California, Los Angeles (UCLA)

Los Angeles, CA

Bachelor of Science in Electrical Engineering (BSEE)

September 2021 – June 2025

Cumulative GPA: 4.00/4.00 | ECE Department Valedictorian 2025 | Fast Track to Success ECE Honors Program

EXPERIENCE

Cellular RF Software Intern

San Diego, CA

Apple Inc.

June 2025 – September 2025

- Developed internal Python tool for converting erroneous cellular field scenario logs into cycle-accurate C++ transceiver tests
- Auto-generated test cases for cellular integration issues enable reproducibility on internal platforms to verify fixes
- Constructed rule-based database for parsing modem AT commands to track RF hardware allocation and timing dependencies
- Productionized via integration with a developer CLI and Jenkins CI for early detection of timing regressions

DSP & Wireless Communications Intern

Irvine, CA

Anduril Industries, Inc.

June 2024 – September 2024

- Optimized detectors for frequency-hopping spread spectrum OFDM signals for 3x greater probability of signal intercept
- Wrote embedded application software in C for radio module control and chirp spread spectrum (CSS) waveform design
- Developed end-to-end RF system test platform to verify and quantify efficacy of jamming waveform designs

Wireless Research Assistant

Los Angeles, CA

Wireless Lab / Networked Embedded Systems Lab, UCLA ECE

February 2022 – June 2025

- Developed mmWave phased array and SDR control platform in Python as lab infrastructure for beamforming experiments
- Implemented range-Doppler radar and IEEE 802.11a (OFDM Wi-Fi) core PHY for joint communication and sensing (JCAS)
- JCAS project for next-generation smart traffic lights awarded \$1.5M in design competition for US Dept of Transportation
- Simulated MAC and PHY layers in MATLAB for networked underwater sensing nodes utilizing acoustic communication
- “LocoMote: AI-driven Sensor Tags for Fine-Grained Undersea Localization and Sensing,” 2nd Author, *IEEE Sensors Journal*

PROJECTS

MIMO-OFDM Receiver Processing on GPU | C++, ArrayFire, Python, Sionna

Jan 2025 – Mar 2025

- Prototyped MIMO-OFDM receiver pipeline on Jetson Nano GPU with ArrayFire / C++
- Implemented OFDM demodulation, least-squares channel estimation, and LMMSE equalization with block-type pilots
- Achieved >20x throughput over Nvidia Sionna and TensorFlow baselines in Python
- Analyzed performance effects on BER vs. Eb/No plots of pilot density and user mobility using 3GPP UMi channel models

FPGA Audio Spectrum Visualizer | SystemVerilog, Intel Quartus Prime

September 2023 – June 2024

- Wrote Cooley-Tukey FFT module with SystemVerilog on Intel FPGA for capturing spectra of microphone input signals
- Developed VGA interface and ping-pong RAM buffering of FFT outputs for smooth 60Hz display of spectrum to a monitor
- Expanded project with signal processing features including Hamming windowing, FIR filtering, and DC offset calibration

From-Scratch Superheterodyne Radio | C, MATLAB, LTspice

September 2022 – June 2023

- Implemented BPSK radio DSP pipeline with Costas Loop carrier recovery and Mueller-Muller timing recovery in MATLAB
- Rewrote application in C for real-time processing on STM32F4 microcontroller with STM32CubeIDE
- Designed and simulated amplifiers, mixers, oscillators, and filters for HF band Tx/Rx superheterodyne radio pair in LTspice

COURSEWORK

Modern Wireless Communications I, II | Numerical Linear Algebra & Optimization | Dynamical Systems | Random Processes

Digital Signal Processing I, II | Audio & Image Processing | Computational Imaging | Deep Learning & Neural Networks

Computer Architecture | Data Structures & Algorithms (C++) | Operating Systems (POSIX, C) | Digital Logic Design

RF Systems | Electromagnetics I, II | Digital Integrated Circuits (Cadence Virtuoso) | VLSI Systems | Analog Integrated Circuits