VYOM GARG

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Driven by a deep curiosity for innovation, I seek opportunities to refine my skills and contribute meaningfully to the evolving landscape of Integrated Circuit design through continuous learning and impactful collaboration.

EDUCATIONAL QUALIFICATIONS

M.S. in Electrical Engineering, Stanford University, California JUN 2026 (Expected)

Coursework: Introduction to VLSI Systems (EE271), Fundamentals of Analog Integrated Circuit Design (EE214A), Product Management for Electrical Engineers and Computer Scientists (EE205)**.**

B.Tech. in Electronics and Communication Engineering, Delhi Technological University, Delhi JUN 2021

Merit Scholarship for Academic Distinction. CGPA: 9.34/10.0

WORK EXPERIENCE

Senior Product Specialist, Ansys Software Private Ltd, Bangalore JAN 2021 – AUG 2024

(Fast Track Promotion for Exceptional Performance)

- **Hardware Security Solutions**:
  - Collaborated with a cross functional team in developing a Pre-Silicon solution to detect vulnerabilities in Crypto Systems against Side-channel and EM Fault Injection Attacks.
  - Conducted simulations of Power-Noise and EM Side Channel effects by probing the victim IC's power grid.
  - Authored the user manual for the Redhawk-SC Security tool, significantly improving customer usability.
- **Productization of SigmaDVD / SigmaAV**: Conducted rigorous testing and analysis of intricate workflows, particularly in sDVD, making substantial contributions to development and evaluation for Tier-1 industry clients.
- **Performance Optimization, Cloud Capability Enhancement and Client-Focused Enablement**
  - Spearheaded initiatives to enable and optimize Ansys tools for cloud-based environments, harnessing the scalability and flexibility of cloud technologies, working closely with R&D teams, field engineers, and cloud resource management to drive the initiative forward.
  - Delivered research findings on optimizing Redhawk-SC for cloud platforms at both Ansys TechCon and Ansys ESCOP enabling cloud capabilities for major clients like ARM,
  - Directed performance enhancements to optimize effectiveness in handling large-scale customer designs.
  - Conducted comprehensive performance and efficiency analysis for Micro Resiliency in Redhawk-SC, contributing to enhanced system resilience and increase the adoption across international customers
- **Hierarchical IR Drop Flow Development**: Led validation, spec design, and prototyping for the hierarchical IR Drop Flow in Redhawk-SC, developing automation utilities in Python that utilized Map Reduce for efficient report analysis.
- **Request Review and Management**:
  - Evaluated approximately 50 requests per release cycle, analyzing customer requirements and conducting surveys to identify key challenges while aligning customer needs with R&D release capabilities.
  - Developed an ADO Dashboard for streamlined tracking of Product Specialist's team triage activities.

INTERNSHIPS

Product Manager Intern at Ambarella SEP 2024 – PRESENT

- Evaluated Ambarella's culture, technology, and development ecosystem to discover key product opportunities, providing strategic insights to leadership.
- Collaborating with cross-functional teams and emerging market players to design a Minimum Viable Product that streamlines workflows, enhances usability, and accelerates integration within Ambarella's hardware ecosystem.

Indian Academy of Sciences, Summer Research Fellow MAY 2020 – AUG 2020

(Supervisor: Prof. Manoj Saxena, Delhi University)

- Utilized Silvaco TCAD to simulate the impact of Total Ionization Dose effects on N-Channel MOSFET and Line TFET based storage elements, gaining insights into their behavior under radiation.
- Concluded that Single Event Upset simulated by Oxygen ions cause temporary deflection in device characteristics but do not result in permanent damage, with the potential for reverting data destruction through refreshing storage elements.

POSITION OF RESPONSIBILITIES

UG Research Assistant, VLSI Research Design Group, DTU FEB 2019 – MAY 2021

- **Innovative Shadow Filtering Technique:** Developed Operational Transconductance Amplifier (OTRA) based shadow filtering method, effectively reducing active elements typically required in standard Bi-quad based Shadow filters.
- **Advanced SRAM Structure Development:** Gained comprehensive knowledge of SRAM cell functionalities and introduced a novel SRAM architecture, enhancing efficiency and reliability.
- **Leadership and Mentorship:**
  - Demonstrated leadership by mentoring and guiding junior students in their projects, facilitating their understanding of research methodologies.
  - Collaborated with senior researchers on experiments and data collection, contributing to significant advancements in the research field.

PUBLICATIONS

- **V. Garg**, V. Goel and N. Pandey, "**A Novel Loadless 6T-SRAM Cell with Isolated Read Port," 2021** *Journal of Physics: Conference Series, First International Conference on Advances in Smart Sensor, Signal Processing and Communication Technology (ICASSCT 2021),* doi: 10.1088/1742-6596/1921/1/012037.
- **V. Garg** and P. Mittal, "**Design and Analysis of LFSR based Content Addressable Memory**," **2021** *International Conference on Computing, Communication, and Intelligent Systems (ICCCIS),* 2021, pp. 935-939, doi: 10.1109/ICCCIS51004.2021.9397071.
- P. Prakash, N. Jayanthi, **V. Garg** and S. Saxena, **"Underwater Image Enhancement: A Review", 2019** *Journal of Emerging Technologies and Innovative Research (JETIR).* https://www.jetir.org/papers/JETIRCO06023.pdf

ACADEMIC PROJECTS

Rasterization Pipeline in C++ and System Verilog OCT 2024 – DEC 2024

- Developed an emulator for the rasterization algorithm, a critical component of the graphics pipeline, using C++.
- Optimized a rasterization unit through iterative improvements, including back face culling, precision reduction, and clock gating, resulting in a 94.99% reduction in Figure of Merit from 297.71 to 14.91
- Implemented techniques for occupied area reduction and frequency scaling, achieving a 41.67% decrease in clock period, 36.71% reduction in total area, and 72.22% decrease in required rasterization units for the desired throughput.

Memory Controller for Multi-level Cache in C++ JUN 2024 – JUL 2024

- Designed a comprehensive memory hierarchy system featuring a controller to support LW & SW operations efficiently.
- The system featured a direct-mapped L1 cache with 16 lines, an 8-way set-associative L2 cache with 2 lines, and a fully associative victim cache for L1 with 4 entries.
- All caches utilized an LRU replacement policy implemented using a linked list data structure in C++.
- Each cache level was exclusive, implemented write-no-allocate and write-through policies

Designing and Implementing RISC-V Simulator in C++ MAY 2024 – JUN 2024

- Developed a RISC-V simulator in C++ capable of executing the RV32I instruction set.
- Modularly implemented processor components as C++ classes, supporting arithmetic, logic, memory, and control flow operations.

A Novel Loadless 6T-SRAM Cell with Isolated Read Port (B.Tech. Capstone Thesis) SEP 2020 – FEB 2021

- Designed a dual-port load-less SRAM structure, utilizing access transistors to establish a feedback loop along with an isolated read port.
- Conducted extensive simulations using HSpice and PTM 32nm Technology node to evaluate the performance and demonstrate significant enhancements with an increase of 84.76% in read margins and 40.81% in write stability.
- Validated the effectiveness of the design, showcasing its potential to enhance the performance of memory systems.

LFSR Based Associative Memory MAR 2020 – JUN 2020

- Designed and implemented an innovative associative memory architecture leveraging the random searching capabilities of a Linear Feedback Shift Register (LFSR) to achieve faster access time and optimized hardware utilization.
- Utilized Icarus Verilog on a remote cloud machine for efficient simulation of the design conducting ~1.3M iterations and verified the results using GTKWave, ensuring accurate functionality and performance.

AWARDS

Global ESOBU Team Excellence Award for enabling Ansys tools on customer cloud environments.	MAR 2024
Global Semiconductor ACE Individual Excellence Award for productizing DataLake and SigmaDVD.	NOV 2023
Legends at Work Award in recognition of teamwork and collaboration.	MAR 2023
Rising Star Award for Excellent performance in First Year at Ansys.	JUL 2022
Best Paper Award for "A Novel Loadless 6T-SRAM Cell with Isolated Read Port" at ICASSCT 2021.	FEB 2021
Merit Scholarship for Department Rank 1 for 3rd year of B.Tech. at DTU.	MAY 2020

RECOGNITIONS

Excellent content and best PS Update Presentation in 2023	DEC 2023
Contributions to SigmaAV & SigmaDVD for Tier-1 clients and other advanced research projects.	DEC 2023
Contributions to work on Data Lake, Triages and 24R1/R2 Reviews and Self-Paced Training.	DEC 2023
Going above and beyond duties and taking ownership of work in Redhawk SC-Security.	DEC 2022
Teamwork and Collaboration for identifying bottlenecks in runtime with Xilinx customers.	NOV 2022
Results and Accountability based on work and presentation on Micro-Resiliency at Ansys.	AUG 2021

TECHNICAL SKILLS

Programming/Scripting Languages: Python, Unix Shell, C/C++, RISC-V Assembly

Hardware Description Languages: Verilog, VHDL

EDA Tools: Cadence PSpice, HSpice, Cadence Virtuoso, Xilinx Vivado, Redhawk-SC, Redhawk-SC Security, GTKWave, Silvaco TCAD