HUI SUB "DAVID" SHIM

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EDUCATION

The University of Texas at Austin — Bachelor of Business Administration, Management Information Systems, High Honors — December 2012
Overall GPA: 3.95; *Major GPA:* 4.00

Bachelor of Arts, Economics, Highest Honors — December 2012
Minor in Mathematics
Economics Major GPA: 3.94, Mathematics Minor GPA: 4.00

WORK EXPERIENCE

Samsung Electronics Memory Division, Software Development Team

Senior Software Engineer, Associate Architect; Hwaseong, Korea — March 2023 – Present

- Developed firmware for NVM Express enterprise solid-state drives supplied to Oracle, Dell EMC, IBM, and HP
- Served as associate architect in defining new modules for metadata management and open time optimization
- Focus: metadata management, open time optimization, NAND flash exception management, power-loss protection

Software Engineer; Hwaseong, Korea — January 2016 – February 2023

- Graduated an intensive 16-month training program designed to provide comprehensive knowledge equivalent to an undergraduate degree in Electrical and Computer Engineering and received the best trainee award
- Developed firmware for NVM Express and SAS enterprise solid-state drives supplied to Dell EMC, IBM, and HP

The University of Texas at Austin IROM Department – *Teaching Assistant;* Austin, TX — Spring 2012 – Fall 2012

- Provided in-depth, personal learning experience for students in a class of over 750 undergraduates through office hours
- Advised undergraduate students of all majors about different sectors and industries in business

The University of Texas at Austin Economics Department – *Research Assistant;* Austin, TX — Spring 2011 – Spring 2012

- Examined spending habits and consumer behavior of over 70 college students to devise a theory
- Published and presented thesis paper on how technology can improve K-12 public education in developing countries

Sanger Learning Center, the University of Texas at Austin – *Supplemental Instruction Leader;* Austin, TX — Fall 2010 – Fall 2011

- Coordinated and led weekly review sessions for an undergraduate microeconomics course of 750 students
- Cooperated in weekly meetings to form a regression equation to prove the effectiveness of the program

Boston Consulting Group – *Summer Intern*; Seoul, Korea — July 2011

- Researched financial reports, cash flow status, and major revenue sources of competitors in the shipbuilding industry
- Analyzed and consolidated business articles in order to provide business strategy and solution

MAJOR PROJECTS AND RESEARCH EXPERIENCE

Samsung Best Paper Contest 2022 — November 2022

- Led the meta block reliability management project and published "STM: Improving the Reliability of SSD through Selective Trim Manager" as the first author
- Striving for increased performance, a device must have maximum over-provisioning and minimum write amplification factor by reducing NAND blocks allocated for metadata, despite associated reliability risks of intensifying wear-out.
- The research addressed device vulnerability to NAND flash errors during extensive programs to metadata blocks, particularly in shutdown and large trim scenarios, by devising two distinct solutions to mitigate each case.
- Shutdown case: In a bid to balance metadata reliability and device open time, we proposed dynamic shutdown manager, which manages the current open range and estimated open time, determining the necessity of a shutdown process. Consequently, if the open time requirement is predicted to be met without a shutdown process, the manager bypasses the shutdown command, thereby shielding the metadata NAND blocks from unnecessary wear-out.
- Large trim case: To mitigate the extensive metadata programs caused by large trims, even in devices devoid of user data, we proposed selective trim manager. This system divides an SSD into several logical zones, managing the valid user data count within each. Upon receiving a trim command, the manager scans the relevant logical zones for valid data and ignores the trim command for empty zones, thereby preventing superfluous metadata programs and bolstering reliability.
- Both the Dynamic Shutdown Manager and Selective Trim Manager were successfully integrated into our end-products, resulting in a significant reduction of metadata wear-outs by more than 25% under normal user workload, and effectively eliminating worst-case scenarios of repeated shutdown and full device trim commands.

Consumer Electronics Show (CES) Innovation Award January 2022

- Received the innovation award by CES 2022 for developing the world's first PCIe Gen5 enterprise SSD (PM1743)
- Enhanced the project by implementing a technique to substitute metadata DRAM cache with a more efficient flash cache
- Addressing the challenge of metadata cache fully loaded on DRAM cache—which necessitated a DRAM size at least 1/1000th of the device size and thus a physical limit to maximum device capacity and increased costs—we developed software techniques to limit DRAM usage while preserving maximum performance.
- Introducing our Partial DRAM solution, we effectively replaced DRAM cache with NAND flash as the final cache. We optimized the NAND flash operation size, enabling cache segmentation into smaller units to maximize cache hit rate. We also divided read and write cache to minimize read latency and completely conceal write latency.
- In an effort to maintain a complete set of metadata on flash while minimizing the required programs, we devised and implemented a 'Dirty Cache Program Scheme'. Unlike the conventional method of sequentially programming all caches, clean or dirty, this approach collects and stores only the dirty metadata cache into flash, thus minimizing the number of clean cache programs to reduce internal workload.
- Partial DRAM solution enabled devices to operate with reduced DRAM, thus facilitating significant cost savings across all enterprise server SSD products and delivering devices with capacities exceeding 32TB to clients.

President's Award for the World's First 32TB SAS Solid-State Drive (PM1643) September 2019

- Honored with the President's Award for developing the world's first 32TB dual-port SAS enterprise SSD
- Optimized device throughput and reduced latency induced by metadata, thereby enhancing overall system performance
- Recognizing that SSD throughput is dictated by available over-provision and write amplification factor, I focused on minimizing blocks utilized for internal purposes including metadata to maximize NAND blocks for user blocks.
- I estimated the lifetime writes and erases on metadata blocks—defining the device's lifespan as 3 drive writes per day (DWPD) for 5 years. By assessing the maximum program and erase cycles, I calculated the minimal number of required metadata blocks. This reduction in metadata blocks resulted in a significant performance boost of 24%.
- I also segmented all metadata management tasks into smaller, atomic units, reducing firmware core waiting times for hardware accelerators and DMA engines. This restructuring resulted in a 30% decrease in latency caused by metadata.

ADDITIONAL EXPERIENCE AND ACTIVITIES

Asian Business Students Association – *Public Relations Director* Fall 2010 – Spring 2011

- Publicized and organized 'Tuesdays with BBA Staff' to start and improve relationship between students and faculty
- Consulted various ways to improve relationships with other organizations to enhance diversity

Deloitte & United Way – *Alternative Spring Break Participant*; Washington D.C., MD March 2011

- Evaluated the public-school systems of Chicago and its needs for the service of Urban Alliance, a non-profit organization which served by increasing high school graduation rate and assisting with post-graduation plans
- Assessed the feasibility of the replication strategy and devised a recommendation according to the client's values

HONORS AND AWARDS

- College of Liberal Arts Dean's Honors List – Summa Cum Laude Fall 2011 – Fall 2012
- Omicron Delta Epsilon Economics Honors Society Fall 2010 – Fall 2012
- University Honors Fall 2009 – Fall 2012
- College of Liberal Arts Dean's Honors List – Magna Cum Laude Spring 2011

ADDITIONAL INFORMATION

Computer Science Skills: C/C++, Embedded System Design, ARM Programming, Software Design and Development, Solid-State Drive System Design, Storage System Design, Java, Python

Firmware Skills: Flash Translation Layer, Metadata Management, NAND Flash Exception Management, NVM Express Gen 4/5, SAS, Semiconductor Engineering, Advanced Trace32 Skills

Languages: English (Bilingual Proficiency), Korean (Native), Chinese (Elementary Proficiency)