PRIYANKA RAINA

Research Interests: Deep Learning Hardware, Hardware/Software Co-design, Domain-Specific Accelerators, Computer Architecture, VLSI Design, Design Productivity, Near-Memory Computing

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profiles.stanford.edu/priyanka-raina/ **https://priyanka-raina.github.io/**

EDUCATION

Massachusetts Institute of Technology

PhD in Electrical Engineering and Computer Science

Jun 2013 – Feb 2018 Cambridge, MA

GPA: 5/5
Thesis: Energy-Efficient Circuits and Systems for Computational Imaging and Vision on Mobile Devices
Advisor: Anantha Chandrakasan

Massachusetts Institute of Technology

S.M. in Electrical Engineering and Computer Science

Sep 2011 – Jun 2013 Cambridge, MA

GPA: 5/5
Thesis: Architectures for Computational Photography
Advisor: Anantha Chandrakasan

Indian Institute of Technology Delhi

B.Tech. in Electrical Engineering

Jul 2007 – Jun 2011 New Delhi, India

GPA = 9.65/10, Department Rank: 1, Institute Rank: 2
Thesis: Transactional Memory Architecture for Multi-core Processors, *Advisor*: Anshul Kumar

AWARDS AND HONORS

Sloan Research Fellowship 2024
NSF CAREER Award 2023
VLSI Best Demo Paper Award 2022
ISSCC Student Research Preview Award 2022
VLSI Best Student Paper Award 2021
Intel 2021 Rising Star Faculty Award 2021
JSSC Best Paper Award 2020
MICRO Best Paper Award 2019
Hellman Fellow, Stanford 2019
Terman Faculty Fellow, Stanford 2018
Raymie Stata TA Award, MIT 2017
Best Young Scientist Paper Award at ESSCIRC 2017
ISSCC Student Research Preview Award 2017
Invited to the Rising Stars Workshop, CMU 2016
Institute Silver Medal for highest GPA in EE, IIT Delhi 2011
Kalpna Chawla Scholarship, IIT Delhi 2011
Bimla Jain Medal for academic excellence, IIT Delhi 2011
Gold Medal at Indian National Chemistry Olympiad 2007
KVPY (Young Scientists) Fellowship 2005
National Talent Search Scholarship 2005

SERVICE AT STANFORD

Committee on Graduate Studies (C-GS) 2020-22
Stanford CS PhD Admissions Committee 2022-23
Stanford EE Student Life Committee Chair 2021-24
Stanford EE Student Life Committee 2019-20

WORK EXPERIENCE

Stanford University

Assistant Professor, Electrical Engineering

Sep 2018 – Present Stanford, CA

Amazon

Amazon Visiting Academic

May 2023 – Present Sunnyvale, CA

NVIDIA Corporation

Visiting Research Scientist, NVIDIA Research

Jan 2018 - Aug 2018 Santa Clara, CA

Intel Corporation

Graduate Research Intern, Intel Labs

Jun 2013 - Aug 2013 Hillsboro, OR

COMMITTEES

President's Council of Advisors on Science and Technology (PCAST) Working Group on Semiconductors 2022

Associate Editor 2023-24
IEEE Journal of Solid-State Circuits (JSSC)

Associate Editor 2023-24
IEEE Solid-State Circuits Letters (SSCL)

Guest Editor 2021
IEEE Micro Special Issue on Hot Chips

Program Chair, Hot Chips 2020

Technical Program Committee 2025
International Solid-State Circuits Conference (ISSCC)

Technical Program Committee 2022-24
Symposium on VLSI Technology and Circuits (VLSI)

Program Committee 2022-23
External Review Committee 2021
International Symposium on Microarchitecture (MICRO)

Technical Program Committee 2022-23
Design, Automation and Test in Europe Conference (DATE)

Program Committee 2022
International Symposium on High-Performance Computer Architecture (HPCA)

Technical Program Committee 2020-22
Design Automation Conference (DAC)

External Review Committee 2021-22
International Symposium on Computer Architecture (ISCA)

Program Committee, tinyML 2021-22

Program Committee 2020
International Conference on Computer Design (ICCD)

Program Committee, Hot Chips 2019, 2020, 2022-24

Program Committee 2020, 2021
Workshop on Open-Source EDA Technology (WOSET)

IEEE Solid State Circuits Society (SSCS) Technical Committee on Open-Source Ecosystem (TC-OSE) 2022-23

PUBLICATIONS

1. **Cascade: An Application Pipelining Toolkit for Coarse-Grained Reconfigurable Arrays**
   Jackson Melchert, Yuchen Mei, Kalhan Koul, Qiaoyi Liu, Mark Horowitz, Priyanka Raina
   IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2024.
2. **MINOTAUR: An Edge Transformer Inference and Training Accelerator with 12 MBytes On-Chip Resistive RAM and Fine-Grained Spatiotemporal Power Gating**
   Kartik Prabhu, Robert M. Radway, Jeffrey Yu, Kai Bartolone, Massimo Giordano, Fabian Peddinghaus, Yonatan Urman, Win-San Khwa, Yu-Der Chih, Meng-Fan Chang, Subhasish Mitra, Priyanka Raina
   IEEE Symposium on VLSI Technology & Circuits (VLSI), June 2024.
3. **Onyx: A 12nm 756 GOPS/W Coarse-Grained Reconfigurable Array for Accelerating Dense and Sparse Applications**
   Kalhan Koul, Maxwell Strange, Jackson Melchert, Alex Carsello, Yuchen Mei, Olivia Hsu, Taeyoung Kong, Po-Han Chen, Huifeng Ke, Keyi Zhang, Qiaoyi Liu, Gedeon Nyengele, Akhilesh Balasingam, Jayashree Adivarahan, Ritvik Sharma, Zhouhua Xie, Christopher Torng, Joel Emer, Fredrik Kjolstad, Mark Horowitz, Priyanka Raina
   IEEE Symposium on VLSI Technology & Circuits (VLSI), June 2024.
4. **EMBER: Efficient Multiple-Bits-per-Cell Embedded RRAM Macro for High-Density Digital Storage**
   Akash Levy, Luke R. Upton, Michael D. Scott, Dennis Rich, Win-San Khwa, Yu-Der Chih, Meng-Fan Chang, Subhasish Mitra, Boris Murmann, Priyanka Raina
   IEEE Journal of Solid-State Circuits (JSSC), 2024.
5. **8-bit Transformer Inference and Fine-tuning for Edge Accelerators**
   Jeffrey Yu, Kartik Prabhu, Yonatan Urman, Robert M. Radway, Eric Han, Priyanka Raina
   ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2024.
6. **Cascade: An Application Pipelining Toolkit for Coarse-Grained Reconfigurable Arrays**
   Jackson Melchert, Yuchen Mei, Kalhan Koul, Qiaoyi Liu, Mark Horowitz, Priyanka Raina
   Languages, Tools, and Techniques for Accelerator Design (LATTE) Workshop at the ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2024.
7. **FastPASE: An AI-Driven Fast PPA Speculation Engine for RTL Design Space Optimization**
   Akash Levy, Joe Walston, Priyanka Raina, Stelios Diamantidis
   International Symposium on Quality Electronic Design (ISQED), April 2024.
8. **Amber: A 16nm System-on-Chip with a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra**
   Kathleen Feng, Taeyoung Kong, Kalhan Koul, Jackson Melchert, Alex Carsello, Qiaoyi Liu, Gedeon Nyengele, Maxwell Strange, Keyi Zhang, Ankita Nayak, Jeff Setter, James Thomas, Kavya Sreedhar, Po-Han Chen, Nikhil Bhagdikar, Zachary Myers, Brandon D'Agostino, Pranil Joshi, Stephen Richardson, Christopher Torng, Mark Horowitz, Priyanka Raina
   IEEE Journal of Solid-State Circuits (JSSC), March 2024. Link
9. **PBA: Percentile-Based Level Allocation for Multiple-Bits-Per-Cell RRAM**
   Anjiang Wei, Akash Levy, Pu Yi, Robert Radway, Priyanka Raina, Subhasish Mitra, Sara Achour
   IEEE/ACM International Conference On Computer Aided Design (ICCAD), October 2023. Link
10. **EMBER: A 100 MHz, 0.86 mm^2, Multiple-Bits-per-Cell RRAM Macro in 40 nm CMOS with Compact Peripherals and 1.0 pJ/bit Read Circuitry**
    Luke R. Upton, Akash Levy, Michael D. Scott, Dennis Rich, Win-San Khwa, Yu-Der Chih, Meng-Fan Chang, Subhasish Mitra, Priyanka Raina, Boris Murmann
    IEEE European Solid-State Circuits Conference (ESSCIRC), September 2023. Link
11. **PEak: A Single Source of Truth for Hardware Design and Verification**
    Caleb Donovick, Ross Daly, Jackson Melchert, Lenny Truong, Priyanka Raina, Pat Hanrahan, Clark Barrett
    Programming Languages for Architecture (PLARCH) Workshop at PLDI, June 2023. Link
12. **An Open-Source 4x8 Coarse-Grained Reconfigurable Array Using SkyWater 130 nm Technology and Agile Hardware Design Flow**
    Po-Han Chen, Charles Tsao, Priyanka Raina
    IEEE International Symposium on Circuits and Systems (ISCAS), May 2023. Link
13. **Canal: A Flexible Interconnect Generator for Coarse-Grained Reconfigurable Arrays**
    Jackson Melchert, Keyi Zhang, Yuchen Mei, Mark Horowitz, Christopher Torng, Priyanka Raina
    IEEE Computer Architecture Letters (CAL), April 2023. Link
14. **Ultra-Dense 3D Physical Design Enables New Architectural Design Points with Large Benefits**
    Tathagata Srimani, Robert M. Radway, Jinwoo Kim, Kartik Prabhu, Dennis Rich, Carlo Gilardi, Priyanka Raina, Max M. Shulaker, Sung-Kyu Lim, Subhasish Mitra
    Conference & Exhibition on Design, Automation & Test in Europe (DATE), April 2023. Link
15. **APEX: A Framework for Automated Processing Element Design Space Exploration using Frequent Subgraph Analysis**
    Jackson Melchert, Kathleen Feng, Caleb Donovick, Ross Daly, Ritvik Sharma, Clark Barrett, Mark Horowitz, Pat Hanrahan, Priyanka Raina
    ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March

2023. Link

16. **3-D Coarse-Grained Reconfigurable Array Using Multi-Pole NEM Relays for Programmable Routing**
Akash Levy, Michael Oduoza, Akhilesh Balasingam, Roger T. Howe, Priyanka Raina
Integration, January 2023. Link
17. **High-Density Analog Image Storage in an Analog-Valued Non-Volatile Memory Array**
Xin Zheng, Ryan V. Zarcone, Akash Levy, Win-San Khwa, Priyanka Raina, Bruno Olshausen, H.-S. Philip Wong
Neuromorphic Computing and Engineering, December 2022. Link
18. **Unified Buffer: Compiling Image Processing and Machine Learning Applications to Push-Memory Accelerators**
Qiaoyi Liu, Jeff Setter, Dillon Huff, Maxwell Strange, Kathleen Feng, Mark Horowitz, Priyanka Raina, Fredrik Kjolstad
ACM Transactions on Architecture and Code Optimization (TACO), November 2022. Link
19. **Synthesizing Instruction Selection Rewrite Rules from RTL using SMT**
Ross Daly, Caleb Donovick, Jack Melchert, Raj Setaluri, Nestan Tsiskaridze, Priyanka Raina, Clark Barrett, Pat Hanrahan
Formal Methods in Computer-Aided Design (FMCAD), October 2022. Link
20. **Canal: A Flexible Interconnect Generator for Coarse-Grained Reconfigurable Arrays**
Jackson Melchert, Keyi Zhang, Yuchen Mei, Mark Horowitz, Christopher Torng, Priyanka Raina
Workshop on Democratizing Domain-Specific Accelerators (WDDSA) at MICRO, October 2022. Link
21. **Hardware Abstractions and Hardware Mechanisms to Support Multi-Task Execution on Coarse-Grained Reconfigurable Arrays**
Taeyoung Kong, Kalhan Koul, Priyanka Raina, Mark A Horowitz, Christopher Torng
Workshop on Democratizing Domain-Specific Accelerators (WDDSA) at MICRO, October 2022. Link
22. **Improving Energy Efficiency of CGRAs with Low-Overhead Fine-Grained Power Domains**
Ankita Nayak, Keyi Zhang, Raj Setaluri, Alex Carsello, Makai Mann, Christopher Torng, Stephen Richardson, Rick Bahr, Pat Hanrahan, Mark Horowitz, Priyanka Raina
ACM Transactions on Reconfigurable Technology and Systems (TRETS), August 2022. Link
23. **A Compute-In-Memory Chip Based on Resistive Random-Access Memory**
Weier Wan, Rajkumar Kubendran, Clemens Schaefer, S. Burc Eryilmaz, Wenqiang Zhang, Dabin Wu, Stephen Deiss, Priyanka Raina, He Qian, Bin Gao, Siddharth Joshi, Huaqiang Wu, H.-S. Philip Wong, Gert Cauwenberghs
Nature, August 2022. Link
24. **Amber: Coarse-Grained Reconfigurable Array-Based SoC for Dense Linear Algebra Acceleration**
Kathleen Feng, Alex Carsello, Taeyoung Kong, Kalhan Koul, Qiaoyi Liu, Jackson Melchert, Gedeon Nyengele, Maxwell Strange, Keyi Zhang, Ankita Nayak, Jeff Setter, James Thomas, Kavya Sreedhar, Po-Han Chen, Nikhil Bhagdikar, Zachary Myers, Brandon D'Agostino, Pranil Joshi, Stephen Richardson, Rick Bahr, Christopher Torng, Mark Horowitz, Priyanka Raina
IEEE Hot Chips Symposium (Hot Chips), August 2022. Link
25. **Enabling Reusable Physical Design Flows with Modular Flow Generators**
Alex Carsello, James Thomas, Ankita Nayak, Po-Han Chen, Mark Horowitz, Priyanka Raina, Christopher Torng
ACM/IEEE Design Automation Conference (DAC), July 2022. Link
26. **Amber: A 367 GOPS, 538 GOPS/W 16nm SoC with a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra**
Alex Carsello, Kathleen Feng, Taeyoung Kong, Kalhan Koul, Qiaoyi Liu, Jackson Melchert, Gedeon Nyengele, Maxwell Strange, Keyi Zhang, Ankita Nayak, Jeff Setter, James Thomas, Kavya Sreedhar, Po-Han Chen, Nikhil Bhagdikar, Zachary Myers, Brandon D'Agostino, Pranil Joshi, Stephen Richardson, Rick Bahr, Christopher Torng, Mark Horowitz, Priyanka Raina
IEEE Symposium on VLSI Technology & Circuits (VLSI), June 2022. Link ***Best Demo Paper Award***
27. **AHA: An Agile Approach to the Design of Coarse-Grained Reconfigurable Accelerators and Compilers**
Kalhan Koul, Jackson Melchert, Kavya Sreedhar, Leonard Truong, Gedeon Nyengele, Keyi Zhang, Qiaoyi Liu, Jeff Setter, Po-Han Chen, Yuchen Mei, Maxwell Strange, Ross Daly, Caleb Donovick, Alex Carsello, Taeyoung Kong, Kathleen Feng, Dillon Huff, Ankita Nayak, Rajsekhar Setaluri, James Thomas, Nikhil Bhagdikar, David Durst, Zachary Myers, Nestan Tsiskaridze, Stephen Richardson, Rick Bahr, Kayvon Fatahalian, Pat Hanrahan, Clark Barrett, Mark Horowitz, Christopher Torng, Fredrik Kjolstad, Priyanka Raina
ACM Transactions on Embedded Computing Systems (TECS), April 2022. Link
28. **An Agile Approach to the Design of Hardware Accelerators and Adaptable Compilers**
Ross Daly, Jackson Melchert, Kalhan Koul, Raj Setaluri, Rick Bahr, Clark Barrett, Nikhil Bhagdikar, Alex Carsello, Caleb Donovick, David Durst, Kayvon Fatahalian, Kathleen Feng, Pat Hanrahan, Teguh Hofstee, Mark Horowitz, Dillon Huff, Fredrik Kjolstad, Taeyoung Kong, Qiaoyi Liu, Makai Mann, Ankita Nayak, Aina Niemetz, Gedeon Nyengele, Stephen Richardson, Jeff Setter, Kavya Sreedhar, Maxwell Strange, James Thomas, Christopher Torng, Leonard Truong, Nestan Tsiskaridze, Keyi Zhang, Priyanka Raina
GOMACTech, March 2022. Link
29. **CHIMERA: A 0.92 TOPS, 2.2 TOPS/W Edge AI Accelerator with 2 MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference**
Kartik Prabhu, Albert Gural, Zainab F. Khan, Robert M. Radway, Massimo Giordano, Kalhan Koul, Rohan Doshi, John W. Kustin, Timothy Liu, Gregorio B. Lopes, Victor Turbiner, Win-San Khwa, Yu-Der Chih, Meng-Fan Chang, Guenole Lallement, Boris Murmann, Subhasish Mitra, Priyanka Raina
IEEE Journal of Solid-State Circuits (JSSC), January 2022. Link

30. **Efficient Routing for Coarse-Grained Reconfigurable Arrays using Multi-Pole NEM Relays**
Akash Levy, Michael Oduoza, Akhilesh Balasingam, Roger T. Howe, Priyanka Raina
IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), January 2022. Link
31. **SAPIENS: A 64-Kbit RRAM-Based Non-Volatile Associative Memory for One-Shot Learning and Inference at the Edge**
Haitong Li, Wei-Chen Chen, Akash Levy, Ching-Hua Wang, Hongjie Wang, Po-Han Chen, Weier Wan, Win-San Khwa, Harry Chuang, Y.-D. Chih, Meng-Fan Chang, H.-S. Philip Wong, Priyanka Raina
IEEE Transactions on Electron Devices (T-ED), September 2021. Link
32. **RADAR: A Fast and Energy-Efficient Programming Technique for Multiple Bits-per-Cell RRAM Arrays**
Binh Q. Le, Akash Levy, Tony F. Wu, Robert M. Radway, E. Ray Hsieh, Xin Zheng, Mark Nelson, Priyanka Raina, H.-S. Philip Wong, Simon Wong, Subhasish Mitra
IEEE Transactions on Electron Devices (T-ED), July 2021. Link
33. **CHIMERA: A 0.92 TOPS, 2.2 TOPS/W Edge AI Accelerator with 2 MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference**
Massimo Giordano, Kartik Prabhu, Kalhan Koul, Robert M. Radway, Albert Gural, Rohan Doshi, Zainab F. Khan, John W. Kustin, Timothy Liu, Gregorio B. Lopes, Victor Turbiner, Win-San Khwa, Yu-Der Chih, Meng-Fan Chang, Guenole Lallement, Boris Murmann, Subhasish Mitra, Priyanka Raina
IEEE Symposium on VLSI Circuits (VLSI), June 2021. Link ***Best Student Paper Award***
34. **One-Shot Learning with Memory-Augmented Neural Networks Using a 64-kbit, 118 GOPS/W RRAM-Based Non-Volatile Associative Memory**
Haitong Li, Wei-Chen Chen, Akash Levy, Ching-Hua Wang, Hongjie Wang, Po-Han Chen, Weier Wan, H.-S. Philip Wong, Priyanka Raina
IEEE Symposium on VLSI Technology (VLSI), June 2021. Link
35. **Simba: Scaling Deep-Learning Inference with Chiplet-Based Architecture**
Yakun Sophia Shao, Jason Cemons, Rangharajan Venkatesan, Brian Zimmer, Matthew Fojtik, Nan Jiang, Ben Keller, Alicia Klinefelter, Nathaniel Pinckney, Priyanka Raina, Stephen G. Tell, Yanqing Zhang, William J. Dally, Joel Emer, C. Thomas Gray, Brucek Khailany, Stephen W. Keckler
Communications of the ACM, June 2021. Link
36. **Automated Codesign of Domain-Specific Hardware Accelerators and Compilers**
Priyanka Raina, Fredrik Kjolstad, Mark Horowitz, Pat Hanrahan, Clark Barrett, Kayvon Fatahalian
ASCR Workshop on Reimagining Codesign, March 2021. Link
37. **Monte Carlo Simulation of a Three-Terminal RRAM with Applications to Neuromorphic Computing**
Akhilesh Balasingam, Akash Levy, Haitong Li, Priyanka Raina
International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), September 2020. Link
38. **Creating an Agile Hardware Design Flow**
Rick Bahr, Clark Barrett, Nikhil Bhagdikar, Alex Carsello, Ross G. Daly, Caleb Donovick, David Durst, Kayvon Fatahalian, Kathleen Feng, Pat Hanrahan, Teguh Hofstee, Mark Horowitz, Dillon Huff, Fredrik Kjolstad, Taeyoung Kong, Qiaoyi Liu, Makai Mann, Jackson Melchert, Ankita Nayak, Aina Niemetz, Gedeon Nyengele, Priyanka Raina, Stephen Richardson, Raj Setaluri, Jeff Setter, Kavya Sreedhar, Maxwell Strange, James Thomas, Christopher Torng, Leonard Truong, Nestan Tsiskaridze, Keyi Zhang
ACM/IEEE Design Automation Conference (DAC), July 2020. Link
39. **A-QED Verification of Hardware Accelerators**
Eshan Singh, Florian Lonsing, Saranyu Chattopadhyay, Maxwell Strange, Peng Wei, Xiaofan Zhang, Yuan Zhou, Deming Chen, Jason Cong, Priyanka Raina, Zhiru Zhang, Clark Barrett, Subhasish Mitra
ACM/IEEE Design Automation Conference (DAC), July 2020. Link
40. **A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing**
Weier Wan, Rajkumar Kubendran, Bin Gao, Siddharth Joshi, Priyanka Raina, Huaqiang Wu, Gert Cauwenberghs, H. S. Philip Wong
IEEE Symposium on VLSI Circuits (VLSI), June 2020. Link
41. **Automating Vitiligo Skin Lesion Segmentation Using Convolutional Neural Networks**
Makena Low, Victor Huang, Priyanka Raina
IEEE International Symposium on Biomedical Imaging (ISBI), April 2020. Link
42. **Interstellar: Using Halide's Scheduling Language to Analyze DNN Accelerators**
Xuan Yang, Mingyu Gao, Qiaoyi Liu, Jeff Setter, Jing Pu, Ankita Nayak, Steven Bell, Kaidi Cao, Heonjae Ha, Priyanka Raina, Christos Kozyrakis, Mark Horowitz
ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2020. Link
43. **A Framework for Adding Low-Overhead, Fine-Grained Power Domains to CGRAs**
Ankita Nayak, Keyi Zhang, Raj Setaluri, Alex Carsello, Makai Mann, Stephen Richardson, Rick Bahr, Pat Hanrahan, Mark Horowitz, Priyanka Raina
Conference & Exhibition on Design, Automation & Test in Europe (DATE), March 2020. Link
44. **A 74 TMACS/W CMOS-ReRAM Neurosynaptic Core with Dynamically Reconfigurable Dataflow and In-Situ Transposable**

Weights for Probabilistic Graphical Models
Weier Wan, Rajkumar Kubendran, S. Burc Eryilmaz, Wenqiang Zhang, Yan Liao, Dabin Wu, Stephen Deiss, Bin Gao, Priyanka Raina, Siddharth Joshi, Huaqiang Wu, Gert Cauwenberghs, H.-S. Philip Wong
IEEE International Solid-State Circuits Conference (ISSCC), February 2020. Link

45. **A 0.32-128 TOPS, Scalable Multi-Chip-Module-based Deep Neural Network Inference Accelerator with Ground-Referenced Signaling in 16nm**
Brian Zimmer, Rangharajan Venkatesan, Yakun Sophia Shao, Jason Clemons, Matthew Fojtik, Nan Jiang, Ben Keller, Alicia Klinefelter, Nathaniel Pinckney, Priyanka Raina, Stephen G. Tell, Yanqing Zhang, William J. Dally, Joel S. Emer, C. Thomas Gray, Stephen W. Keckler, Brucek Khailany
IEEE Journal of Solid-State Circuits (JSSC), January 2020. Link ***JSSC Best Paper Award***
46. **MAGNet: A Modular Accelerator Generator for Neural Networks**
Rangharajan Venkatesan, Yakun Sophia Shao, Miaorong Wang, Jason Clemons, Steve Dai, Matthew R. Fojtik, Ben Keller, Alicia Klinefelter, Nathaniel Ross Pinckney, Priyanka Raina, Yanqing Zhang, Brian Zimmer, William J. Dally, Joel S. Emer, Stephen W. Keckler, Brucek Khailany
IEEE/ACM International Conference On Computer Aided Design (ICCAD), November 2019. Link
47. **Simba: Scaling Deep-Learning Inference with Multi-Chip-Module-Based Architecture**
Yakun Sophia Shao, Jason Clemons, Rangharajan Venkatesan, Brian Zimmer, Matthew Fojtik, Nan Jiang, Ben Keller, Alicia Klinefelter, Nathaniel Pinckney, Priyanka Raina, Stephen G. Tell, Yanqing Zhang, William J. Dally, Joel Emer, C. Thomas Gray, Brucek Khailany, Stephen W. Keckler
IEEE/ACM International Symposium on Microarchitecture (MICRO), October 2019. Link ***Best Paper Award, Top Picks in Computer Architecture Honorable Mentions***
48. **Neuro-Inspired Computing with Emerging Memories: Where Device Physics Meets Learning Algorithms**
Haitong Li, Priyanka Raina, H.-S. Philip Wong
Proceedings of SPIE, September 2019. Link
49. **Creating An Agile Hardware Flow**
Rick Bahr, Clark Barrett, Nikhil Bhagdikar, Alex Carsello, Nate Chizgi, Ross G. Daly, Caleb Donovick, David Durst, Kayvon Fatahalian, Kathleen Feng, Pat Hanrahan, Teguh Hofstee, Mark Horowitz, Dillon Huff, Taeyoung Kong, Zheng Liang, Qiaoyi Liu, Makai Mann, Zachary Alexander Myers, Ankita Nayak, Aina Niemetz, Gedeon Nyengele, Priyanka Raina, Stephen Richardson, Raj Setaluri, Jeff Setter, Daniel Stanley, Maxwell Strange, Charles Tsao, James Thomas, Leonard Truong, Xuan Yang, Keyi Zhang
IEEE Hot Chips Symposium (Hot Chips), August 2019. Link
50. **A 0.11 pJ/Op, 0.32-128 TOPS, Scalable Multi-Chip-Module-based Deep Neural Network Accelerator Designed with a High-Productivity VLSI Methodology**
Rangharajan Venkatesan, Yakun Sophia Shao, Brian Zimmer, Jason Clemons, Matthew Fojtik, Nan Jiang, Ben Keller, Alicia Klinefelter, Nathaniel Pinckney, Priyanka Raina, Stephen G. Tell, Yanqing Zhang, William J. Dally, Joel S. Emer, C. Thomas Gray, Stephen W. Keckler, Brucek Khailany
IEEE Hot Chips Symposium (Hot Chips), August 2019. Link
51. **A 0.11 pJ/Op, 0.32-128 TOPS, Scalable Multi-Chip-Module-based Deep Neural Network Accelerator with Ground-Reference Signaling in 16nm**
Brian Zimmer, Rangharajan Venkatesan, Yakun Sophia Shao, Jason Clemons, Matthew Fojtik, Nan Jiang, Ben Keller, Alicia Klinefelter, Nathaniel Pinckney, Priyanka Raina, Stephen G. Tell, Yanqing Zhang, William J. Dally, Joel S. Emer, C. Thomas Gray, Stephen W. Keckler, Brucek Khailany
IEEE Symposium on VLSI Circuits (VLSI), June 2019. Link
52. **Timeloop: A Systematic Approach to DNN Accelerator Evaluation**
Angshuman Parashar, Priyanka Raina, Yakun Sophia Shao, Yu-Hsin Chen, Victor A. Ying, Anurag Mukkara, Rangharajan Venkatesan, Brucek Khailany, Stephen W. Keckler, Joel Emer
IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2019. Link
53. **An Energy-Scalable Accelerator for Blind Image Deblurring**
Priyanka Raina, Mehul Tikekar, Anantha P. Chandrakasan
IEEE Journal of Solid-State Circuits (JSSC), July 2017. Link
54. **An Energy-Scalable Accelerator for Blind Image Deblurring**
Priyanka Raina, Mehul Tikekar, Anantha P. Chandrakasan
IEEE European Solid-State Circuits Conference (ESSCIRC), September 2016. Link ***Best Young Scientist Paper Award***
55. **A 0.6V 8mW 3D Vision Processor for a Navigation Device for the Visually Impaired**
Dongsuk Jeon, Nathan Ickes, Priyanka Raina, Hsueh-Cheng Wang, Daniela Rus, Anantha Chandrakasan
IEEE International Solid-State Circuits Conference (ISSCC), February 2016. Link
56. **Reconfigurable Processor for Energy-Efficient Computational Photography**
Rahul Rithe, Priyanka Raina, Nathan Ickes, Srikanth V. Tenneti, Anantha P. Chandrakasan
IEEE Journal of Solid-State Circuits (JSSC), November 2013. Link
57. **Reconfigurable Processor for Energy-Scalable Computational Photography**
Rahul Rithe, Priyanka Raina, Nathan Ickes, Srikanth V. Tenneti, Anantha P. Chandrakasan
IEEE International Solid-State Circuits Conference (ISSCC), February 2013. Link

PREPRINTS

1. **PEak: A Single Source of Truth for Hardware Design and Verification**
   Caleb Donovick, Ross Daly, Jackson Melchert, Lenny Truong, Priyanka Raina, Pat Hanrahan, Clark Barrett
   February 2024. Link
2. **Efficiently Synthesizing Lowest Cost Rewrite Rules for Instruction Selection**
   Ross Daly, Caleb Donovick, Jackson Melchert, Priyanka Raina, Clark Barrett, Pat Hanrahan,
   May 2023.

TEACHING

Course descriptions can be found here: https://priyanka-raina.github.io/teaching/.

1. **Design Projects in VLSI Systems - I (EE272)**
   Stanford, *Instructor*, Students: 44 — Winter 2024
2. **Emerging Non-Volatile Memory Devices and Circuit Design (EE309B)**
   Stanford, *Instructor*, Students: 10 — Winter 2024
3. **Semiconductor Memory Devices and Circuit Design (EE309A)**
   Stanford, *Instructor*, Students: 19 — Autumn 2023
4. **Design Projects in VLSI Systems - II (EE372)**
   Stanford, *Instructor*, Students: 9 — Spring 2023
5. **Design Projects in VLSI Systems - I (EE272)**
   Stanford, *Instructor*, Students: 27 — Winter 2023
6. **Introduction to VLSI Systems (EE271)**
   Stanford, *Instructor*, Students: 61 — Autumn 2022
7. **Design Projects in VLSI Systems - II (EE372)**
   Stanford, *Instructor*, Students: 14 — Spring 2022
8. **Design Projects in VLSI Systems - I (EE272)**
   Stanford, *Instructor*, Students: 33 — Winter 2022
9. **Emerging Non-Volatile Memory Devices and Circuit Design (EE309B)**
   Stanford, *Instructor*, Students: 6 — Winter 2022
10. **Introduction to VLSI Systems (EE271)**
    Stanford, *Instructor*, Students: 49 — Autumn 2021
11. **Semiconductor Memory Devices and Circuit Design (EE309A)**
    Stanford, *Instructor*, Students: 10 — Autumn 2021
12. **Design Projects in VLSI Systems - II (EE272B)**
    Stanford, *Instructor*, Students: 14 — Spring 2021
13. **Design Projects in VLSI Systems - I (EE272A)**
    Stanford, *Instructor*, Students: 26 — Winter 2021
14. **Emerging Non-Volatile Memory Devices and Circuit Design (EE309B)**
    Stanford, *Instructor*, Students: 10 — Winter 2021
15. **Semiconductor Memory Devices and Circuit Design (EE309A)**
    Stanford, *Instructor*, Students: 28 — Autumn 2020
16. **Design Projects in VLSI Systems (EE272)**
    Stanford, *Instructor*, Students: 21 — Winter 2020
17. **Introduction to VLSI Systems (EE271)**
    Stanford, *Instructor*, Students: 36 — Autumn 2019
18. **Design Projects in VLSI Systems (EE272)**
    Stanford, *Instructor*, Students: 37 — Winter 2019
19. **Introduction to VLSI Systems (EE271)**
    Stanford, *Instructor*, Students: 44 — Autumn 2018
20. **Analysis and Design of Digital Integrated Circuits (6.374)**
    MIT, *Instructor*, Students: 7 — Fall 2017
21. **Preparation for Undergraduate Research (6.UAR)**
    MIT, *Head Teaching Assistant*, Students: 142 — Spring 2017
22. **Preparation for Undergraduate Research (6.UAR)**
    MIT, *Teaching Assistant*, Students: 179 — Fall 2015
23. **Introduction to EECS (6.01)**
    MIT, *Teaching Assistant*, Students: 491 — Spring 2014
24. **Analog Electronics (EEL204)**
    IIT Delhi, *Teaching Assistant*, Students: 100 — Spring 2011

PRESENTATIONS

1. **Agile Hardware Design (AHA): An Overview**
   Stanford University and University of Tokyo Workshop on Agile and Low-Cost Hardware Design for the Domain-Specific Computing Era — April 22, 2024
2. **MINOTAUR: 8-bit Posit-Based Transformer Inference and Fine-tuning Accelerator for Edge Applications**
   SystemX Alliance 2024 Spring Workshop on the Intersection of AI, Edge, and Sensing Systems — April 16, 2024
3. **Agile Design of Domain-Specific Accelerators and Compilers**
   University of Pennsylvania Electrical and Systems Engineering (ESE) Colloquium — October 3, 2023
4. **Looking Ahead - ML Systems in 10 Years**
   Google ML and Systems Rising Stars Workshop Panel — August 18, 2023
5. **Agile Design of Domain-Specific Accelerators and Compilers**
   Solid-State Circuits Society (SSCS) Technical Webinar — July 14, 2023
6. **High Level Synthesis: Now is the time or will it continue to remain just a promising technology?**
   Design Automation Conference (DAC) Panel — July 13, 2023
7. **Agile Co-design of Domain-Specific Accelerators and Compilers**
   Design Automation Conference (DAC) — July 12, 2023
8. **Deep Neural Network Acceleration Using Resistive RAM Based Near-Memory Computing**
   Design Automation Conference (DAC) — July 12, 2023
9. **CHIMERA: Efficient DNN Inference and Training at the Edge with On-Chip Resistive RAM**
   International Symposium on Integrated Circuits and Systems for Smart Society — June 16, 2023
10. **MINOTAUR: Transformer Inference and Training at the Edge with Posits and RRAM**
    ACCESS Technology Symposium on "Frontiers of AI Accelerators: Technologies, Circuits and Applications" — June 5, 2023
11. **Hardware Accelerator for Enabling High-Performance AI on Tiny Edge Devices**
    SRC AI Hardware (AIHW) Meeting at IBM Almaden — May 24, 2023
12. **MINOTAUR: Transformer Inference and Training at the Edge with Posits and RRAM**
    JUMP 2.0 CoCoSys Meeting at Georgia Institute of Technology — May 17, 2023
13. **Agile Design of Domain-Specific Accelerators and Compilers**
    University of Southern California Seminar — March 30, 2023
14. **Agile Design of Domain-Specific Accelerators and Compilers**
    Cornell University Seminar — March 23, 2023
15. **Agile Design of Domain-Specific Accelerators and Compilers**
    University of California, Los Angeles Seminar — March 20, 2023
16. **Co-design of Programmable Hardware Accelerators and Compilers for Future Heterogeneous Computing Systems**
    International Solid-State Circuits Conference (ISSCC) Forum on The Future of Heterogeneous Multi-core Architectures for AI and Other Specialized Processing — February 23, 2023
17. **Agile Design of Domain-Specific Accelerators and Compilers**
    Princeton University Seminar — February 15, 2023
18. **Agile Design of Domain-Specific Accelerators and Compilers**
    University of California, Berkeley Seminar — January 31, 2023
19. **App Store for Hardware**
    Intel Heterogeneous Integrated Platforms (HIP) Workshop — December 9, 2022
20. **Agile Design of Domain-Specific Accelerators and Compilers**
    SLICE Seminar at University of California, Berkeley — November 9, 2022
21. **Agile Design of Domain-Specific Accelerators and Compilers**
    Keynote presentation at Synopsys Engineering Leadership Conference — October 27, 2022
22. **AHA: An Agile Approach to the Design of Programmable Accelerators and Compilers**
    Samsung Seminar — September 22, 2022
23. **AHA: An Agile Approach to the Design of Programmable Accelerators and Compilers**
    Samsung Seminar — September 5, 2022
24. **AHA: An Agile Approach to the Design of Reconfigurable Accelerators and Compilers**
    Google ACRS Workshop — August 16, 2022
25. **VLSI Curriculum Development and Sharing**
    Apple NSI HBCU Workshop — August 2, 2022
26. **AHA: An Agile Approach to the Design of Coarse-Grained Reconfigurable Accelerators and Compilers**
    Cisco Seminar — July 6, 2022
27. **Design of a Fully-Integrated Multiple-Bits-per-Cell RRAM Macro**
    ACCESS Seminar — May 19, 2022
28. **Accelerating Semiconductor Innovation in the U.S.**

PCAST Public Meeting on the Challenges and Opportunities for U.S. Leadership in Semiconductors (Link) May 12, 2022

29. **AHA: An Agile Approach to the Design of Coarse-Grained Reconfigurable Accelerators and Compilers**
Berkeley/Stanford/UCSC Cloud Workshop (Link) May 11, 2022
30. **Agile Hardware-Compiler Co-design for Domain-Specific Accelerators**
Intel Seminar April 7, 2022
31. **CHIMERA: Efficient DNN Inference and Training at the Edge with On-Chip Resistive RAM**
Intel Rising Star Tech Talk March 30, 2022
32. **CHIMERA: Efficient DNN Training and Inference at the Edge with On-Chip Resistive RAM**
3rd Workshop on Accelerator CAD (co-located with ICCAD 2021) November 5, 2021
33. **CHIMERA: Efficient DNN Training and Inference at the Edge with On-Chip Resistive RAM**
Rutgers Efficient AI Seminar (Link) October 21, 2021
34. **How Computer Chips Get Speedier Through Specialization**
Stanford Engineering's The Future of Everything podcast with Russ Altman (Link) September 21, 2021
35. **CHIMERA: Efficient DNN Inference at the Edge with On-Chip Resistive RAM**
Cirrus Logic Seminar August 3, 2021
36. **CHIMERA: Efficient DNN Inference at the Edge with On-Chip Resistive RAM**
ACCESS Seminar July 1, 2021
37. **Agile Hardware-Compiler Codesign for Domain-Specific Accelerators**
Intel Seminar June 21, 2021
38. **Automated Codesign of Domain-Specific Hardware Accelerators and Compilers**
ASCR Workshop on Reimagining Codesign March 17, 2021
39. **Creating an Agile Hardware Accelerator Design Flow**
2nd Workshop on Accelerator CAD (co-located with ICCAD 2020) November 6, 2020
40. **Convex Optimization for Hardware Constrained Neural Networks**
Facebook AI Systems Faculty Summit October 6, 2020
41. **Agile Design of Domain-Specific Architectures**
AI Hardware Summit September 30, 2020
42. **Creating an Agile Hardware Design Flow**
Google Brain Seminar August 5, 2020
43. **Agile Design of Domain-Specific Architectures**
Computer Forum August 2, 2020
44. **Creating an Agile Hardware Design Flow**
Design Automation Conference (DAC) July 22, 2020
45. **Creating an Agile Hardware Accelerator Design Flow**
Computer Science Department Seminar, University of Oxford November 27, 2019
46. **Creating an Agile Hardware Accelerator Design Flow**
1st Workshop on Accelerator CAD (co-located with ICCAD 2019) November 7, 2019
47. **Creating an Agile Hardware Flow**
DARPA ERI Summit July 17, 2019
48. **Leveraging Embedded NVMs in Accelerator Architectures**
AMD Seminar May 7, 2019
49. **Agile Hardware Design – Enabling Rapid Hardware/Software Systems Design for AI of Things**
Intel PSG Seminar April 17, 2019
50. **Agile Hardware Design – Enabling Rapid Hardware/Software Systems Design for AI of Things**
CASPA 2019 Spring Symposium March 9, 2019
51. **Hardware Accelerators for Computational Imaging and Machine Learning**
SCIEN Industry Affiliates Meeting November 30, 2018
52. **Hardware Accelerators for Computational Imaging and Machine Learning**
Apple Seminar November 16, 2018
53. **Hardware Accelerators for Computational Imaging and Machine Learning**
SystemX Fall Conference November 14, 2018
54. **Energy-Efficient Circuits and Systems for Computational Imaging and Vision on Mobile Devices**
Solid-State Circuits Society (SSCS) Distinguished Lecturer Talk (Link) October 18, 2018
55. **Energy-Efficient Circuits and Systems for Computational Imaging and Vision on Mobile Devices**
Computer Forum Seminar April 10, 2018
56. **Energy-Efficient Circuits and Systems for Computational Imaging and Vision on Mobile Devices**
Stanford SystemX Seminar March 8, 2018