Priyanka Raina

Contact Information

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Education

Massachusetts Institute of Technology (MIT) — Jun 2013 - Feb 2018
PhD in Electrical Engineering and Computer Science (EECS) — GPA: 5.0/5.0
Thesis: Energy-Efficient Circuits and Systems for Computational Imaging and Vision on Mobile Devices
Committee: Anantha Chandrakasan (advisor), Vivienne Sze, Arvind
Minor: Cognitive Science

Massachusetts Institute of Technology (MIT) — Sep 2011 - Jun 2013
S.M. in Electrical Engineering and Computer Science — GPA: 5.0/5.0
Thesis: Architectures for Computational Photography
Advisor: Anantha Chandrakasan

Indian Institute of Technology (IIT) Delhi — Jul 2007 - May 2011
B.Tech. in Electrical Engineering — GPA: 9.65/10.0
Thesis: Transactional Memory Architecture for Multi-core Processors
Advisor: Anshul Kumar
Department Rank: 1, Institute Rank: 2

Research Interests

Digital Circuit Design, Embedded Systems, Computational Imaging, Computer Vision, Machine Learning, Autonomous Systems, Hardware/Software Co-design, Design Productivity

Work Experience

Stanford University, Stanford — Sep 2018 - Present
Assistant Professor, Electrical Engineering

Nvidia Corporation, Santa Clara — Jan 2018 - Aug 2018
Visiting Research Scientist, Architecture Research Group, Nvidia Research

Intel Corporation, Hillsboro — Jun 2013 - Aug 2013
Graduate Research Intern, Intel Labs

McKinsey & Company, New Delhi — May 2011 - Aug 2011
Business Analyst

The Royal Bank of Scotland, New Delhi — May 2010 - Jul 2010
Summer Intern, Structured Rates Group

Publications

A-QED Verification of Hardware Accelerators
E. Singh, F. Lonsing, S. Chattopadhyay, M. Strange, P. Wei, X. Zhang, Y. Zhao, J. Cong, D. Chen, Z. Zhang, P. Raina, C. Barrett, S. Mitra
Design Automation Conference (DAC), July 2020.

A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing
W. Wan, R. Kubendran, B. Gao, S. Joshi, P. Raina, H. Wu, G. Cauwenberghs, H.-S.

P. Wong
Symposium on VLSI Circuits (VLSI), June 2020.

Automating Vitiligo Skin Lesion Segmentation Using Convolutional Neural Networks
M. Low, P. Raina
IEEE International Symposium on Biomedical Imaging (ISBI), April 2020.

Using Halide's Scheduling Language to Analyze DNN Accelerators
X. Yang, M. Gao, Q. Liu, J. Pu, A. Nayak, J. Setter, S. Bell, K. Cao, H. Ha, P. Raina, C. Kozyrakis, M. Horowitz
International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2020.

A Framework for Adding Low-Overhead, Fine-Grained Power Domains to CGRAs
A. Nayak, K. Zhang, R. Setaluri, A. Carsello, M. Mann, S. Richardson, R. Bahr, P. Hanrahan, M. Horowitz, P. Raina
Design, Automation and Test in Europe Conference (DATE), March 2020.

A 74TMACS/W CMOS-ReRAM Neurosynaptic Core with Dynamically Reconfigurable Dataflow and In-Situ Transposable Weights for Probabilistic Graphical Models
W. Wan, R. Kubendran, S. B. Eryilmaz, W. Zhang, Y. Liao, D. Wu, S. Deiss, B. Gao, P. Raina, S. Joshi, H. Wu, G. Cauwenberghs, H.-S.P. Wong
International Solid-State Circuits Conference (ISSCC), February 2020.

A 0.32-128 TOPS, Scalable Multi-Chip-Module-based Deep Neural Network Inference Accelerator with Ground-Referenced Signaling in 16nm
B. Zimmer, R. Venkatesan, S. Shao, J. Clemons, M. Fojtik, N. Jiang, B. Keller, A. Klinefelter, N. Pinckney, P. Raina, S. G. Tell, Y. Zhang, W. J. Dally, J. S. Emer, C. T. Gray, S. W. Keckler, B. Khailany
Journal of Solid-State Circuits (JSSC), January 2020.

MAGNet: A Modular Accelerator Generator for Neural Networks
R. Venkatesan, S. Shao, M. Wang, J. Clemons, S. Dai, M. Fojtik, B. Keller, A. Klinefelter, N. Pinckney, P. Raina, Y. Zhang, B. Zimmer, B. Dally, J. Emer, S. Keckler, B. Khailany
International Conference On Computer Aided Design (ICCAD), November 2019.

Simba: Scaling Deep-Learning Inference with Multi-Chip-Module-Based Architecture
S. Shao, J. Clemons, R. Venkatesan, B. Zimmer, M. Fojtik, N. Jiang, B. Keller, A. Klinefelter, N. Pinckney, P. Raina, S. Tell, Y. Zhang, B. Dally, J. Emer, C. T. Gray, B. Khailany, S. Keckler
International Symposium on Microarchitecture (MICRO), October 2019. **Best Paper Award, Top Picks in Computer Architecture Honorable Mentions**

Neuro-Inspired Computing with Emerging Memories: Where Device Physics Meets Learning Algorithms
H. Li, P. Raina, H.-S.P. Wong
Proceedings of SPIE, September 2019. (Invited)

Creating An Agile Hardware Flow

R. Bahr, C. Barrett, N. Bhagdikar, A. Carsello, N. Chizgi, R. G. Daly, C. Donovick, D. Durst, K. Fatahalian, P. Hanrahan, T. Hofstee, M. Horowitz, D. Huff, T. Kong, Q. Liu, M. Mann, A. Nayak, A. Niemetz, G. Nyengele, S. Richardson, R. Setaluri, J. Setter, D. Stanley, M. Strange, J. Thomas, L. Truong, X. Yang, K. Zhang, P. Raina
Hot Chips: A Symposium on High Performance Chips (HotChips), August 2019.

A 0.11 pJ/Op, 0.32-128 TOPS, Scalable Multi-Chip-Module-based Deep Neural Network Accelerator Designed with a High-Productivity VLSI Methodology
B. Khailany, R. Venkatesan, Y. S. Shao, B. Zimmer, J. Clemons, M. Fojtik, N. Jiang, B. Keller, A. Klinefelter, N. Pinckney, P. Raina, S. G. Tell, Y. Zhang, W. J. Dally, J. S. Emer, C. T. Gray, S. W. Keckler
Hot Chips: A Symposium on High Performance Chips (HotChips), August 2019.

A 0.11 pJ/Op, 0.32-128 TOPS, Scalable Multi-Chip-Module-based Deep Neural Network Accelerator with Ground-Reference Signaling in 16nm
B. Zimmer, R. Venkatesan, Y. S. Shao, J. Clemons, M. Fojtik, N. Jiang, B. Keller, A. Klinefelter, N. Pinckney, P. Raina, S. G. Tell, Y. Zhang, W. J. Dally, J. S. Emer, C. T. Gray, S. W. Keckler, B. Khailany
Symposium on VLSI Circuits (VLSI), June 2019.

Timeloop: A Systematic Approach to DNN Accelerator Evaluation
A. Parashar, P. Raina, S. Shao, A. Mukkara, V. A. Ying, R. Venkatesan, Y. H. Chen, B. Khailany, S. Keckler, J. Emer
International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2019.

An Energy-Scalable Accelerator for Blind Image Deblurring
P. Raina, M. Tikekar, and A. P. Chandrakasan
Journal of Solid-State Circuits (JSSC), July 2017. (Invited)

An Energy-Scalable Accelerator for Blind Image Deblurring
P. Raina, M. Tikekar, and A. P. Chandrakasan
European Solid-State Circuits Conference (ESSCIRC), September 2016. **Best Student Paper**

A 0.6V 8mW 3D Vision Processor for a Navigation Device for the Visually Impaired
D. Jeon, N. Ickes, P. Raina, H. C. Wang, A. P. Chandrakasan
International Solid-State Circuits Conference (ISSCC), February 2016.

Reconfigurable Processor for Energy-Efficient Computational Photography
R. Rithe, P. Raina, N. Ickes, S. V. Tenneti, A. P. Chandrakasan
Journal of Solid-State Circuits (JSSC), November 2013.

Reconfigurable Processor for Energy-Scalable Computational Photography
R. Rithe, P. Raina, N. Ickes, S. V. Tenneti, A. P. Chandrakasan
International Solid-State Circuits Conference (ISSCC), February 2013.

Publications Under Review

Creating an Agile Hardware Design Flow
R. Bahr, C. Barrett, N. Bhagdikar, A. Carsello, R. Daly, C. Donovick, D. Durst, K. Fatahalian, K. Feng, P. Hanrahan, T. Hofstee, M. Horowitz, D. Huff, F. Kjolstad, T. Kong, Q. Liu, M. Mann, J. Melchert, A. Nayak, A. Niemetz, G. Nyengele, P. Raina,

S. Richardson, R. Setaluri, J. Setter, K. Sreedhar, M. Strange, J, Thomas, C. Torng, L. Truong, N. Tsiskaridze, K. Zhang
Design Automation Conference (DAC), July 2020.

Teaching Experience

Design Projects in VLSI Systems (EE272), Stanford — Winter 2020
Instructor — Students: 21

Introduction to VLSI Systems (EE271), Stanford — Autumn 2019
Instructor — Students: 36

Design Projects in VLSI Systems (EE272), Stanford — Winter 2019
Instructor — Students: 37

Introduction to VLSI Systems (EE271), Stanford — Autumn 2018
Instructor — Students: 44

Analysis and Design of Digital Integrated Circuits (6.374), MIT — Fall 2017
Instructor — Students: 7

Completed a semester-long **Teaching Certificate Program** at MIT — Spring 2014

Preparation for Undergraduate Research (6.UAR), MIT — Spring 2017
Head Teaching Assistant (Instructor: Anantha Chandrakasan) — Students: 142

Preparation for Undergraduate Research (6.UAR), MIT — Fall 2015
Teaching Assistant (Instructor: Anantha Chandrakasan) — Students: 179

Introduction to EECS (6.01), MIT — Spring 2014
Teaching Assistant (Instructor: Leslie Kaelbling) — Students: 491

Analog Electronics (EEL204), IIT Delhi — Spring 2011
Undergraduate Teaching Assistant (Instructor: Shouri Chatterjee) — Students: 100

Committees

Stanford EE Student Life Committee — 2019-20
Technical Program Committee and Session Chair, International Conference on Computer Design (ICCD) — 2020
Program Chair, Hot Chips: A Symposium on High Performance Chips — 2020
Technical Program Committee and Session Chair, Design Automation Conference (DAC) — 2020
Technical Program Committee and Session Chair, Hot Chips: A Symposium on High Performance Chips — 2019
Session Chair, Design Automation Conference (DAC) — 2018

Awards, Honors and Scholarships

Hellman Fellow, Stanford — 2019
Raymie Stata TA Award, MIT — 2017
Awarded the **Best Young Scientist Paper Award at ESSCIRC 2016** for the paper "Energy-Scalable Accelerator for Blind Image Deblurring" — 2017
Awarded the **2016 ISSCC Student Research Preview Award** for "Energy-Scalable Accelerator for Blind Image Deblurring" — 2017
Invited to the **Rising Stars** workshop for women pursuing academic careers — 2016
Institute Silver Medal for highest GPA in Electrical Enginering, IIT Delhi — 2011
Kalpna Chawla Scholarship for undergraduate research, IIT Delhi — 2011

Bimla Jain Medal for academic excellence, IIT Delhi 2011
Gold Medal at Indian National Chemistry Olympiad (InChO) 2007
KVPY (Young Scientists) Fellowship by Indian Institute of Science 2005
National Talent Search Scholarship by NCERT, India 2005

Presentations

Creating an Agile Hardware Accelerator Design Flow, University of Oxford Seminar Nov 2019

Creating an Agile Hardware Accelerator Design Flow, 1st ACCAD Workshop at ICCAD Nov 2019

Creating an Agile Hardware Flow, DARPA ERI Summit Jul 2019

Agile Hardware Design - Enabling Rapid Hardware/Software Systems Design for AI of Things, CASPA 2019 Spring Symposium Mar 2019

Hardware Accelerators for Computational Imaging and Machine Learning, SCIEN Industry Affiliates Meeting Nov 2018

Hardware Accelerators for Computational Imaging and Machine Learning, SystemX Fall Conference Nov 2018

Energy-Efficient Circuits and Systems for Computational Imaging and Vision on Mobile Devices, Solid-State Circuits Society (SSCS) Distinguished Lecturer Talk Oct 2018

Energy-Efficient Circuits and Systems for Computational Imaging and Vision on Mobile Devices, Stanford Computer Forum Apr 2018

Energy-Efficient Circuits and Systems for Computational Imaging and Vision on Mobile Devices, SystemX Seminar Mar 2018