Saleh Kargarrazi

Address: Aeronautics and Astronautics, Stanford University
496 Lomita Mall, Durand Building, Room 202 Stanford, CA 94305-4035
Cell Phone: +1 669-273-9990
E-mail: skargar@stanford.edu

EDUCATION:

- **Ph.D** in Information and Communication Technology
  Royal Institute of Technology (KTH), Stockholm, Sweden, 2011 – 2017.
- **Teknologie Licentiat** in Information and Communication Technology
  Royal Institute of Technology (KTH), Stockholm, Sweden, Dec 2014.
- **M.Sc.** in System-on-Chip Design
  Royal Institute of Technology (KTH), Stockholm, Sweden, 2008 – 2010.
- **B.Sc.** in Electrical Engineering (Electronics)
  Ferdowsi University of Mashhad, Mashhad, Iran, 2003 – 2008.

PUBLICATIONS:

- Journal papers
  - ***(J1)* A study on positive-feedback configuration of a bipolar SiC high temperature operational amplifier**
    Saleh Kargarrazi, Luigia Lanni, Carl-Mikael Zetterling.
    in Solid-State Electronics, vol. 116, pp. 33-37, 2016.
  - ***(J2)* 500 °C Bipolar SiC Linear Voltage Regulator**
    Saleh Kargarrazi, Luigia Lanni, Stefano Saggini, Ana Rusu, Carl-Mikael Zetterling.
    in IEEE Transactions on Electron Devices, vol. 62, no. 6, pp. 1953-1957, 2015.
  - ***(J3)* Design and Characterization of 500 °C Schmitt trigger in 4H-SiC**
    Saleh Kargarrazi, Luigia Lanni, Carl-Mikael Zetterling.
    in Materials Science Forum, vol. 821-823, pp. 897-901, 2015
  - ***(J4)* Bipolar integrated circuits in SiC for extreme environment operation**
    Carl-Mikael Zetterling, Anders Hallen, Raheleh Hedayati, Saleh Kargarrazi, Luigia Lanni, Gunnar Malm, Shabnam Mardani, Hans Norström, Ana Rusu, Sethu Suvanam, Ye Tian, Mikael Östling.
    in Semiconductor Science and Technology, 2016.
  - ***(J5)* 500 °C High Current 4H-SiC Lateral BJTs for High-Temperature Integrated Circuits**
    Hossein Elahipanah, Saleh Kargarrazi, Arash Salemi, Mikeal Östling, Carl-Mikael Zetterling.
    in IEEE Electron Device Letters, vol.38, pp. 1429-1432, 2017.
  - ***(J6)* 500 °C, High Current Linear Voltage Regulator in 4H-SiC BJT Technology**
    Saleh Kargarrazi, Hossein Elahipanah, Saul Rodriguez, Carl-Mikael Zetterling.
    in IEEE Electron Device Letters, vol.39, pp. 548-551, 2018.
- Conference papers (peer-reviewed)

- **High Temperature Passive Components for Extreme Environments**
  Juan Colmenares, Saleh Kargarrazi, Hossein Elahipanah , Hans-Peter Nee, Carl-Mikael Zetterling.
  in 4th IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA).
- **A Monolithic SiC Drive Circuit for SiC Power BJTs**
  Saleh Kargarrazi, Luigia Lanni, Ana Rusu, Carl-Mikael Zetterling.
  in IEEE 27^{th} International Symposium On Power Semiconductor Devices & IC's (ISPSD), 2015, pp. 285-288.
- **Design and Characterization of 500 °C Schmitt trigger in 4H-SiC**
  Saleh Kargarrazi, Luigia Lanni, Carl-Mikael Zetterling.
  in European Conference on Silicon Carbide and Related Materials, 2014 (The same content is published in *J3*).
- **A Metaheuristic Approach for an Optimized Design of a Silicon Carbide Operational Amplifier**
  Maryam Pourreza, Saleh Kargarrazi.
  in 14^{th} International Conference on Integral Methods in Science and Engineering (IMSE), 2016.

- Thesis
  - **High Temperature Bipolar SiC Power Integrated Circuits**
    Ph.D. Thesis, KTH, Stockholm, 2017.
    http://urn.kb.se/resolve?urn=urn:nbn:se:kth:diva-201618
  - **Bipolar Silicon Carbide Integrated Circuits for High Temperature Power Applications**
    Licentiate Thesis, KTH, Stockholm, 2014.
    http://urn.kb.se/resolve?urn=urn:nbn:se:kth:diva-156212
  - **Thermal management on Component Package Level with Thermoelectric (Peltier) Coolers**
    Master Thesis, Ericsson, Stockholm, 2011 (Archived as an Ericsson internal report).

Awards:

- Awarded post-doc fellowship grant by **Knut and Alice Wallenberg foundation**, 2017.
- Winner of the **KTH innovation** annual challenge *Digital Future*. Sweden, December 2016.
- Winner of the **Ericsson AB** business case competition for an existing mobile phone product. Sweden, June 2010. and awarded an internship to implement the business concept on-site, Ericsson, Shanghai, October 2010.
- Awarded the **EURODOTS** scholarship to attend the summer course Power Management", EPFL, Switzerland, 2012.
- Awarded the **Backmarks** travel stipend, to present a paper at ECSCRM, France, 2014

Memberships:

- **IEEE**
  - Student member 2010-present
- **POETS (Center for Power Optimization of Electro-thermal Systems)**
  - 2017- present
- **Vice-chair at IEEE-KTH student branch**

– 2015- 2016

Work Experience:

- **PhD-research**
  - Except fabrication, I contributed to all the stages of high-temperature SiC ICs including device modeling, design, layout and high-temperature measurement. The ICs I designed during my PhD studies were *operational amplifiers, comparators, Schmitt triggers, drivers fo power switches, linear voltage regulators, and integrated control system for switched converters*. 2011- 2017
- **IC designer and layout engineer**
  - Contribute to the PLL design in 65-nm bulk CMOS and layout design for biCMOS and CMOS chipsets. Catena Wireless Electronics (acquired by NXP), Sweden, 2011
- **IC designer**
  - Design of a programmable divider for a fractional-N PLL of a GNSS reciever chipset in 65-nm bulk CMOS, Kisel Microelectronics (acquired by Imagination Technologies), 2010-2011
- **Intern-researcher**
  - Investigating thermoelectric cooling for heat removal from hot-spot (80-120 °C) BGA and QFN chip packages, 2010-2011
- **Digital designer**
  - Contribute to various digital design projects using FPGA (from hard-disk interface design to transparent encyption systems) and consulting start-ups, 2006-2007

Teaching and Mentoring:

- Mentoring two student, EE REU program, Stanford, CA, USA, 2018
- Mentoring a high school teacher, Ignited RET program, Stanford, CA, USA, 2018
- Guest lecturer, *High Frequency Magnetics*,Teacher: Prof. Juan Rivas, Stanford, CA, USA, 2018
- Lab assistant for *Analog Electronics*, Teacher: Bengt Molin. KTH, Sweden, 2013-2014
- Lab assistant for *Digital Logic Design*, Teacher: Prof. Jalil Chitizadeh. FUM, Iran, 2005-2006

Skills:

- Experience in designing various integrated circuits (A/D converters, amplifiers, PLL, oscillator, drivers for power switches, DC-DC converters,...)
- +8 years experience in using Cadence IC design/layout tools.
- +5 years experience in using device characterization tools and high temperature measurements.
- Skilled in using simulation and modeling Software (ADS, PSPICE, ICCAP, ADS and Matlab).
- Skilled in coding in C, VHDL, Verilog, Assembly, cadence SKILL.
- Familiar with semiconductor fabrication process and basic experience in working with clean-room facilities (wafer cleaning, lithography, etching, passivation and metalization.)
- Fluent in English, Persian and Swedish.

Favorites:

- Writing short stories and poems, Ice-skating, swimming.