Stanford

Clark Barrett

Professor (Research) of Computer Science

Curriculum Vitae available Online

Bio

BIO

Clark Barrett joined Stanford University as an Associate Professor (Research) of Computer Science in September 2016. Before that, he was an Associate Professor of Computer Science at the Courant Institute of Mathematical Sciences at New York University. His expertise is in constraint solving and its applications to system verification and security. His PhD dissertation introduced a novel approach to constraint solving now known as Satisfiability Modulo Theories (SMT). Today, he is recognized as one of the world's experts in the development and application of SMT techniques. He was also an early pioneer in the development of formal hardware verification: at Intel, he collaborated on a novel theorem prover used to verify key microprocessor properties; and at 0-in Design Automation (now part of Mentor Graphics), he helped build one of the first industrially successful assertion-based verification tool-sets for hardware. He is an ACM Distinguished Scientist.

ACADEMIC APPOINTMENTS

- Professor (Research), Computer Science

ADMINISTRATIVE APPOINTMENTS

- Visiting Scientist, Google, (2015-2017)

HONORS AND AWARDS

- First place (CoSA2 model checker), Hardware Model Checking Competition (HWCC) (2019)
- Best Short Paper for "p4pktgen: Automated Test-Case Generation for P4 Programs", Symposium on Software Defined Networking Research (SOSR) (2018)
- Distinguished Artifact Award for "EMME: A Formal Tool for ECMAScript Memory Model Evaluation", Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS) (2018)
- Best Paper for "Lazy Proofs for DPLL(T)-Based SMT Solvers", International Conference on Formal Methods in Computer-Aided Design (FMCAD) (2016)
- Best Paper for "A Structured Approach to Post-Silicon Validation and Debug using Symbolic QED", IEEE International Test Conference (ITC) (2015)
- Distinguished Scientist, ACM (2014)
- HVC Award, Haifa Verification Conference (2010)
- Software Quality Innovation Award, IBM (2008)
- CAREER award, National Science Foundation (2007)
- Best Paper for "A Decision Procedure for Bit-vector Arithmetic", Design Automation Conference (DAC) (1998)

PROFESSIONAL EDUCATION

- Ph.D., Stanford University , Computer Science (2003)

PATENTS

- Subhasish Mitra, Clark Barrett, David Lin, Eshan Singh. "United States Patent 10528448 Post-silicon Validation and Debug using Symbolic Quick Error Detection", The Board of Trustees of the Leland Stanford Junior University (Palo Alto, CA, US); New York University (New York, NY, US), Jan 7, 2020

Research & Scholarship

CURRENT RESEARCH AND SCHOLARLY INTERESTS

In an increasingly automated and networked world, one of the most pressing challenges we face is ensuring the security and dependability of hardware and software systems. Formal techniques (based on mathematical logic and automated reasoning) are among the most powerful tools available for finding difficult bugs and ensuring correctness. Unfortunately, formal methods today either require extensive manual effort or are severely limited in their scope or scalability. My research vision is to develop general-purpose, automated, and scalable formal techniques, with the aim of providing a sound and practical foundation for reliable computer systems.

The starting point for this vision is a new class of logical engines based on Satisfiability Modulo Theories (SMT)}, an emerging research area I helped found as part of my PhD dissertation in 2003. My research agenda focuses on advancing the theory, implementation, and applications of SMT. The primary vehicle for this research is an open-source SMT solver called CVC4 (see cvc4.cs.stanford.edu). Some current applications of SMT that my group is working on include automatically finding bugs in hardware and software, automatically finding security vulnerabilities, and automatically verifying the safety of autonomous controllers generated using machine learning.

PROJECTS

- CVC4 (9/1/2009 - present)

Teaching

STANFORD ADVISEES

Doctoral Dissertation Reader (AC)

Jason Koenig, Wonyeol Lee, Chelsea Sidrane, Eshan Singh

Postdoctoral Faculty Sponsor

Gereon Kremer, Andres Notzli, Aleksandar Zeljic

Doctoral Dissertation Co-Advisor (AC)

Caleb Donovick

Master's Program Advisor

Joanna Yang

Doctoral (Program)

Hanna Lachnitt, Alex Ozdemir, Ying Sheng, Scott Viteri, Amalee Wilson, Haoze Wu

Publications

PUBLICATIONS

- **Reluplex: a calculus for reasoning about deep neural networks** *FORMAL METHODS IN SYSTEM DESIGN*
  Katz, G., Barrett, C., Dill, D. L., Julian, K., Kochenderfer, M. J.
  2021
- **Towards Satisfiability Modulo Parametric Bit-vectors** *JOURNAL OF AUTOMATED REASONING*
  Niemetz, A., Preiner, M., Reynolds, A., Zohar, Y., Barrett, C., Tinelli, C.

2021

- **On solving quantified bit-vector constraints using invertibility conditions** *FORMAL METHODS IN SYSTEM DESIGN*
  Niemetz, A., Preiner, M., Reynolds, A., Barrett, C., Tinelli, C.
  2021
- **Pono: A Flexible and Extensible SMT-Based Model Checker**
  Mann, M., Irfan, A., Lonsing, F., Yang, Y., Zhang, H., Brown, K., Gupta, A., Barrett, C., Silva, A., Leino, K. R.
  SPRINGER INTERNATIONAL PUBLISHING AG.2021: 461-474
- **DeepCert: Verification of Contextually Relevant Robustness for Neural Network Image Classifiers**
  Paterson, C., Wu, H., Grese, J., Calinescu, R., Pasareanu, C. S., Barrett, C., Habli, Sujan, M., Bitsch, F.
  SPRINGER INTERNATIONAL PUBLISHING AG.2021: 3-17
- **Politeness and Stable Infiniteness: Stronger Together**
  Sheng, Y., Zohar, Y., Ringeissen, C., Reynolds, A., Barrett, C., Tinelli, C., Platzer, A., Sutcliffe, G.
  SPRINGER INTERNATIONAL PUBLISHING AG.2021: 148-165
- **Gap-free Processor Verification by S(2)QED and Property Generation**
  Devarajegowda, K., Fadiheh, M., Singh, E., Barrett, C., Mitra, S., Ecker, W., Stoffel, D., Kunz, W., DiNatale, G., Bolchini, C., Vatajelu, E. I.
  IEEE.2020: 526–31
- **Towards Verification of Neural Networks for Small Unmanned Aircraft Collision Avoidance**
  Irfan, A., Julian, K. D., Wu, H., Barrett, C., Kochenderfer, M. J., Meng, B., Lopez, J., IEEE
  IEEE.2020
- **The Move Prover**
  Zhong, J., Cheang, K., Qadeer, S., Grieskamp, W., Blackshear, S., Park, J., Zohar, Y., Barrett, C., Dill, D. L., Lahiri, S. K., Wang, C.
  SPRINGER INTERNATIONAL PUBLISHING AG.2020: 137-150
- **fault: A Python Embedded Domain-Specific Language for Metaprogramming Portable Hardware Verification Components** *International Conference on Computer Aided Verification*
  Truong, L., Herbst, S., Setaluri, R., Mann, M., Daly, R., Zhang, K., Donovick, C., Stanley, D., Horowitz, M., Barrett, C., Hanrahan, P.
  2020
- **Creating an Agile Hardware Design Flow**
  Bahr, R., Barrett, C., Bhagdikar, N., Carsello, A., Daly, R., Donovick, C., Durst, D., Fatahalian, K., Feng, K., Hanrahan, P., Hofstee, T., Horowitz, M., Huff, et al
  IEEE.2020
- **A-QED Verification of Hardware Accelerators**
  Singh, E., Lonsing, F., Chattopadhyay, S., Strange, M., Wei, P., Zhang, X., Zhou, Y., Chen, D., Cong, J., Raina, P., Zhang, Z., Barrett, C., Mitra, et al
  IEEE.2020
- **Selected Extended Papers of NFM 2017: Preface** *JOURNAL OF AUTOMATED REASONING*
  Barrett, C., Kahsai, T.
  2019; 63 (4): 1003–4
- **Refutation-based synthesis in SMT** *FORMAL METHODS IN SYSTEM DESIGN*
  Reynolds, A., Kuncak, V., Tinelli, C., Barrett, C., Deters, M.
  2019; 55 (2): 73–102
- **Reports of the AAAI 2019 Spring Symposium Series** *AI MAGAZINE*
  Baldini, I., Barrett, C., Chella, A., Cinelli, C., Gamez, D., Gilpin, L. H., Hinkelmann, K., Holmes, D., Kido, T., Kocaoglu, M., Lawless, W. F., Lomuscio, A., Macbeth, et al
  2019; 40 (3): 59–66
- **Verifying Deep-RL-Driven Systems**
  Kazak, Y., Barrett, C., Katz, G., Schapira, M., Assoc Comp Machinery
  ASSOC COMPUTING MACHINERY.2019: 83–89
- **G2SAT: Learning to Generate SAT Formulas.** *Advances in neural information processing systems*

You, J. n., Wu, H. n., Barrett, C. n., Ramanujan, R. n., Leskovec, J. n.
2019; 32: 10552–63

- **Unlocking the Power of Formal Hardware Verification with CoSA and Symbolic QED**
  Lonsing, F., Ganesan, K., Mann, M., Nuthakki, S., Singh, E., Srouji, M., Yang, Y., Mitra, S., Barrett, C., IEEE
  IEEE.2019
- **CVC4SY: Smart and Fast Term Enumeration for Syntax-Guided Synthesis**
  Reynolds, A., Barbosa, H., Notzli, A., Barrett, C., Tinelli, C., Dillig, Tasiran, S.
  SPRINGER INTERNATIONAL PUBLISHING AG.2019: 74–83
- **High-Level Abstractions for Simplifying Extended String Constraints in SMT**
  Reynolds, A., Notzli, A., Barrett, C., Tinelli, C., Dillig, Tasiran, S.
  SPRINGER INTERNATIONAL PUBLISHING AG.2019: 23–42
- **The Marabou Framework for Verification and Analysis of Deep Neural Networks**
  Katz, G., Huang, D. A., Ibeling, D., Julian, K., Lazarus, C., Lim, R., Shah, P., Thakoor, S., Wu, H., Zeljic, A., Dill, D. L., Kochenderfer, M. J., Barrett, et al
  SPRINGER INTERNATIONAL PUBLISHING AG.2019: 443–52
- **Integration and Flight Test of Small UAS Detect and Avoid on A Miniaturized Avionics Platform**
  Lopez, J. G., Ren, L., Meng, B., Fisher, R., Markham, J., Figard, M., Evans, R., Spoelhof, R., Rubenstahl, M., Edwards, S., Pedan, I., Barrett, C., IEEE
  IEEE.2019
- **Invertibility Conditions for Floating-Point Formulas**
  Brain, M., Niemetz, A., Preiner, M., Reynolds, A., Barrett, C., Tinelli, C., Dillig, Tasiran, S.
  SPRINGER INTERNATIONAL PUBLISHING AG.2019: 116–36
- **G2SAT: Learning to Generate SAT Formulas**
  You, J., Wu, H., Barrett, C., Ramanujan, R., Leskovec, J., Wallach, H., Larochelle, H., Beygelzimer, A., d'Alche-Buc, F., Fox, E., Garnett, R.
  NEURAL INFORMATION PROCESSING SYSTEMS (NIPS).2019
- **Processor Hardware Security Vulnerabilities and their Detection by Unique Program Execution Checking**
  Fadiheh, M., Stoffel, D., Barrett, C., Mitra, S., Kunz, W., IEEE
  IEEE.2019: 994–99
- **Symbolic QED Pre-silicon Verification for Automotive Microcontroller Cores: Industrial Case Study**
  Singh, E., Devarajegowda, K., Simon, S., Schnieder, R., Ganesan, K., Fadiheh, M., Stoffel, D., Kunz, W., Barrett, C., Ecker, W., Mitra, S., IEEE
  IEEE.2019: 1000–1005
- **Symbolic Quick Error Detection Using Symbolic Initial State for Pre-Silicon Verification**
  Fadiheh, M., Urdahl, J., Nuthakki, S., Mitra, S., Barrett, C., Stoffel, D., Kunz, W., IEEE
  IEEE.2018: 55–60
- **Solving Quantified Bit-Vectors Using Invertibility Conditions**
  Niemetz, A., Preiner, M., Reynolds, A., Barrett, C., Tinelli, C., Chockler, H., Weissenbacher, G.
  SPRINGER INTERNATIONAL PUBLISHING AG.2018: 236–55
- **p4pktgen: Automated Test Case Generation for P4 Programs**
  Notzli, A., Khan, J., Fingerhut, A., Barrett, C., Athanas, P., ACM
  ASSOC COMPUTING MACHINERY.2018
- **CoSA: Integrated Verification for Agile Hardware Design**
  Mattarei, C., Mann, M., Barrett, C., Daly, R. G., Huff, D., Hanrahan, P., Bjorner, N., Gurfinkel, A.
  IEEE.2018: 7–11
- **REASONING WITH FINITE SETS AND CARDINALITY CONSTRAINTS IN SMT** *LOGICAL METHODS IN COMPUTER SCIENCE*
  Bansal, K., Barrett, C., Reynolds, A., Tinelli, C.
  2018; 14 (4)
- **EMME: A Formal Tool for ECMAScript Memory Model Evaluation**
  Mattarei, C., Barrett, C., Guo, S., Nelson, B., Smith, B., Beyer, D., Huisman, M.

SPRINGER INTERNATIONAL PUBLISHING AG.2018: 55–71

- **Datatypes with Shared Selectors**
  Reynolds, A., Viswanathan, A., Barbosa, H., Tinelli, C., Barrett, C., Galmiche, D., Schulz, S., Sebastiani, R.
  SPRINGER INTERNATIONAL PUBLISHING AG.2018: 591–608
- **Constraint solving for finite model finding in SMT solvers** *THEORY AND PRACTICE OF LOGIC PROGRAMMING*
  Reynolds, A., Tinelli, C., Barrett, C.
  2017; 17 (4): 516–58
- **Relational Constraint Solving in SMT**
  Meng, B., Reynolds, A., Tinelli, C., Barrett, C., DeMoura, L.
  SPRINGER INTERNATIONAL PUBLISHING AG.2017: 148–65
- **Designing Theory Solvers with Extensions**
  Reynolds, A., Tinelli, C., Jovanovic, D., Barrett, C., Dixon, C., Finger, M.
  SPRINGER INTERNATIONAL PUBLISHING AG.2017: 22–40
- **Partitioned Memory Models for Program Analysis**
  Wang, W., Barrett, C., Wies, T., Bouajjani, A., Monniaux, D.
  SPRINGER INTERNATIONAL PUBLISHING AG.2017: 539–58
- **E-QED: Electrical Bug Localization During Post-silicon Validation Enabled by Quick Error Detection and Formal Methods**
  Singh, E., Barrett, C., Mitra, S., Majumdar, R., Kuncak
  SPRINGER INTERNATIONAL PUBLISHING AG.2017: 104–25
- **Reluplex: An Efficient SMT Solver for Verifying Deep Neural Networks**
  Katz, G., Barrett, C., Dill, D. L., Julian, K., Kochenderfer, M. J., Majumdar, R., Kuncak
  SPRINGER INTERNATIONAL PUBLISHING AG.2017: 97–117
- **Scaling Up DPLL(T) String Solvers Using Context-Dependent Simplification**
  Reynolds, A., Woo, M., Barrett, C., Brumley, D., Liang, T., Tinelli, C., Majumdar, R., Kuncak
  SPRINGER INTERNATIONAL PUBLISHING AG.2017: 453–74
- **Towards Proving the Adversarial Robustness of Deep Neural Networks** *ELECTRONIC PROCEEDINGS IN THEORETICAL COMPUTER SCIENCE*
  Katz, G., Barrett, C., Dill, D. L., Julian, K., Kochenderfer, M. J.
  2017: 19–26
- **Symbolic Quick Error Detection for Pre-Silicon and Post-Silicon Validation: Frequently Asked Questions** *IEEE DESIGN & TEST*
  Singh, E., Lin, D., Barrett, C., Mitra, S.
  2016; 33 (6): 55-62
- **An efficient SMT solver for string constraints** *FORMAL METHODS IN SYSTEM DESIGN*
  Liang, T., Reynolds, A., Tsiskaridze, N., Tinelli, C., Barrett, C., Deters, M.
  2016; 48 (3): 206–34
- **Lazy Proofs for DPLL(T)-Based SMT Solvers**
  Katz, G., Barrett, C., Tinelli, C., Reynolds, A., Hadarean, L., Piskac, R., Talupur, M.
  IEEE.2016: 93–100
- **Efficient solving of string constraints for security analysis**
  Barrett, C., Tinelli, C., Deters, M., Liang, T., Reynolds, A., Tsiskaridze, N., ACM
  ASSOC COMPUTING MACHINERY.2016: 4–6
- **Structured Approach to Post-Silicon Validation and Debug Using Symbolic Quick Error Detection**
  Lin, D., Singh, E., Barrett, C., Mitra, S., IEEE
  IEEE.2015
- **A Decision Procedure for Regular Membership and Length Constraints over Unbounded Strings**
  Liang, T., Tsiskaridze, N., Reynolds, A., Tinelli, C., Barrett, C., Lutz, C., Ranise, S.

SPRINGER-VERLAG BERLIN.2015: 135–50

- **Fine Grained SMT Proofs for the Theory of Fixed-Width Bit-Vectors**
  Hadarean, L., Barrett, C., Reynolds, A., Tinelli, C., Deters, M., Davis, M., Fehnker, A., McIver, A., Voronkov, A.
  SPRINGER INT PUBLISHING AG.2015: 340–55
- **Cascade 2.0**
  Wang, W., Barrett, C., Wies, T., McMillan, K. L., Rival
  SPRINGER-VERLAG BERLIN.2014: 142–60
- **6 Years of SMT-COMP** *JOURNAL OF AUTOMATED REASONING*
  Barrett, C., Deters, M., de Moura, L., Oliveras, A., Stump, A.
  2013; 50 (3): 243–77
- **Being careful about theory combination** *FORMAL METHODS IN SYSTEM DESIGN*
  Jovanovic, D., Barrett, C.
  2013; 42 (1): 67-90
- **The Design and Implementation of the Model Constructing Satisfiability Calculus**
  Jovanovic, D., Barrett, C., de Moura, L., IEEE
  IEEE.2013: 173–80
- **Witness Runs for Counter Machines**
  Barrett, C., Demri, S., Deters, M., Galmiche, D., LarcheyWendling, D.
  SPRINGER-VERLAG BERLIN.2013: 1–4
- **Witness Runs for Counter Machines**
  Barrett, C., Demri, S., Deters, M., Fontaine, P., Ringeissen, C., Schmidt, R. A.
  SPRINGER-VERLAG BERLIN.2013: 120–50
- **Simplex with Sum of Infeasibilities for SMT**
  King, T., Barrett, C., Dutertre, B., IEEE
  IEEE.2013: 189–96
- **Sharing Is Caring: Combination of Theories**
  Jovanovic, D., Barrett, C., Tinelli, C., SofronieStokkermans
  SPRINGER-VERLAG BERLIN.2011: 195–210
- **The SMT-LIB Initiative and the Rise of SMT (HVC 2010 Award Talk)**
  Barrett, C., de Moura, L., Ranise, S., Stump, A., Tinelli, C., Barner, S., Harris, Kroening, D., Raz, O.
  SPRINGER-VERLAG BERLIN.2011: 3
- **Polite Theories Revisited**
  Jovanovic, D., Barrett, C., Fermuller, C. G., Voronkov, A.
  SPRINGER-VERLAG BERLIN.2010: 402–16
- **Verifying Low-Level Implementations of High-Level Datatypes**
  Conway, C. L., Barrett, C., Touili, T., Cook, B., Jackson, P.
  SPRINGER-VERLAG BERLIN.2010: 306–20
- **Solving quantified verification conditions using satisfiability modulo theories** *ANNALS OF MATHEMATICS AND ARTIFICIAL INTELLIGENCE*
  Ge, Y., Barrett, C., Tinelli, C.
  2009; 55 (1-2): 101–22
- **Satisfiability Modulo Theories** *HANDBOOK OF SATISFIABILITY*
  Barrett, C., Sebastiani, R., Seshia, S. A., Tinelli, C., Biere, A., Heule, M., VanMaaren, H., Walsh, T.
  2009; 185: 825–85
- **DESIGN AND RESULTS OF THE 3RD ANNUAL SATISFIABILITY MODULO THEORIES COMPETITION (SMT-COMP 2007)** *INTERNATIONAL JOURNAL ON ARTIFICIAL INTELLIGENCE TOOLS*
  Barrett, C., Deters, M., Oliveras, A., Stump, A.

2008; 17 (4): 569-606

- **Pointer analysis, conditional soundness, and proving the absence of errors** *STATIC ANALYSIS*
  Conway, C. L., Dams, D., Namjoshi, K. S., Barrett, C.
  2008; 5079: 62-77
- **Design and results of the 2nd annual satisfiability modulo theories competition (SMT-COMP 2006)** *FORMAL METHODS IN SYSTEM DESIGN*
  Barrett, C., de Moura, L., Stump, A.
  2007; 31 (3): 221-239
- **CVC3 - (Tool paper)** *COMPUTER AIDED VERIFICATION, PROCEEDINGS*
  Barrett, C., Tinelli, C.
  2007; 4590: 298-302
- **Cascade: C assertion checker and deductive engine (Tool paper)** *COMPUTER AIDED VERIFICATION, PROCEEDINGS*
  Sethi, N., Barrett, C.
  2006; 4144: 166-169
- **Design and results of the first satisfiability modulo theories competition (SMT-COMP 2005)** *JOURNAL OF AUTOMATED REASONING*
  Barrett, C., de Moura, L., Stump, A.
  2005; 35 (4): 373-390
- **TVOC: A translation validator for optimizing compilers** *COMPUTER AIDED VERIFICATION, PROCEEDINGS*
  Barrett, C., Fang, Y., Goldberg, B., Hu, Y., Pnueli, A., Zuck, L.
  2005; 3576: 291-295
- **CVC Lite: A new implementation of the cooperating validity checker** *COMPUTER AIDED VERIFICATION*
  Barrett, C., Berezin, S.
  2004; 3114: 515-518
- **A generalization of Shostak's method for combining decision procedures** *4th International Workshop on Frontiers of Combining Systems*
  Barrett, C. W., Dill, D. L., Stump, A.
  SPRINGER-VERLAG BERLIN.2002: 132–146
- **A framework for cooperating decision procedures** *17th International Conference on Automated Deduction (CADE-17)*
  Barrett, C. W., Dill, D. L., Stump, A.
  SPRINGER-VERLAG BERLIN.2000: 79–98
- **A decision procedure for bit-vector arithmetic** *35th Design Automation Conference*
  Barrett, C. W., Dill, D. L., LEVITT, J. R.
  ASSOC COMPUTING MACHINERY.1998: 522–527
- **Validity checking for combinations of theories with equality** *1st International Conference on Formal Methods in Computer-Aided Design (FMCAD 96)*
  Barrett, C., Dill, D., LEVITT, J.
  SPRINGER-VERLAG BERLIN.1996: 187–201