

# Stanford

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## Jim Plummer

John M. Fluke Professor of Electrical Engineering and Professor, by courtesy, of Materials Science and Engineering

### CONTACT INFORMATION

- **Alternate Contact**

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### Bio

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#### BIO

Jim Plummer was born in Toronto, Canada. He obtained his BS degree from UCLA and his MS and PhD degrees in Electrical Engineering from Stanford University. After graduating from Stanford, he worked as a research staff member in the Integrated Circuits Lab at Stanford for several years before joining the Stanford faculty in 1978 as an associate professor. He became professor of electrical engineering in 1983.

His career at Stanford has included serving as director of the IC Laboratory, senior associate dean in the School of Engineering, and chair of the Electrical Engineering Department. He was the Frederick Emmons Terman Dean of the School of Engineering from 1999 until 2014. He also holds the John Fluke Professorship in Electrical Engineering. During his tenure as dean, the school renewed or replaced much of its laboratory and classroom space, dramatically increased the number of undergraduate students majoring in engineering and created interdisciplinary programs like the Bioengineering Department, which is jointly operated with the medical school, ICME, the Institute For Computational and Mathematical Engineering, and the Hasso Plattner Institute of Design (d.school) that changed the nature of engineering education. Plummer was a strong advocate as dean, for ensuring that engineering majors take advantage of the full set of opportunities at a liberal arts institution like Stanford.

Plummer has worked in a variety of areas in the broad field of silicon devices and technology. Much of his early work focused on high-voltage ICs and on high-voltage device structures. He and his group made important contributions to integrating CMOS logic and high-voltage lateral DMOS devices on the same chip and demonstrated circuits operating at several hundred volts. This work also led to several power MOS device concepts such as the IGBT which have become important power switching devices.

Throughout the 1980s and '90s, a major focus of his work was on silicon process modeling. This work involved many students and other faculty, particularly Professor Bob Dutton, and resulted in the development of several generations of SUPREM, which has become the standard process modeling tool used worldwide today. His recent work has focused on nanoscale silicon devices for logic and memory and has demonstrated new device concepts such as the TRAM thyristor based memory cell and the IMOS device which achieves  $<kT/q$  subthreshold slopes. His recent work has also focused on power devices using wide bandgap semiconductor materials.

Plummer is a member of the National Academy of Engineering, the American Academy of Arts and Sciences and a fellow of the IEEE. He has received many awards for his research, including the 1991 Gordon Moore medal for Solid State Science and Technology from the Electrochemical Society, the 2001 Semiconductor Industry Association University Research Award, the 2003 IEEE J. J. Ebers Award, the 2003 IEEE Van der Ziel Award, the 2007 IEEE Andrew Grove award and the 2015 IEEE Founders Award. He has been elected to the Silicon Valley and ISPSD Halls of Fame.

He has graduated more than 90 PhD students with whom he has published more than 400 journal papers and conference presentations. These papers have won eight conference and student best paper awards including two at IEDM and three at ISSCC. His textbook, "Silicon VLSI Technology: Fundamentals, Practice and Modeling," is used by many universities around the world. He has also received three teaching awards at Stanford. He has served and currently serves on the Board of Directors of several public companies including Intel and Cadence.

Plummer directed the Stanford Nanofabrication Facility from 1994 to 2000 and received an NSF commendation in 2000 for national leadership in building the NNUN, a consortium of universities who opened their nanofabrication facilities as national resources for industry and for students from around the nation.

### **ACADEMIC APPOINTMENTS**

- Professor, Electrical Engineering
- Professor (By courtesy), Materials Science and Engineering
- Member, Bio-X
- Affiliate, Precourt Institute for Energy

### **ADMINISTRATIVE APPOINTMENTS**

- Frederick Emmons Terman Dean, Stanford School of Engineering, (1999-2014)
- Chair, Electrical Engineering Dept., (1996-1999)

### **HONORS AND AWARDS**

- Best Paper Awards, ISSCC (1970, 1976, 1978)
- ASSU Award for Teaching Excellence, ASSU (1991)
- Solid State Science & Technology Award, Society (1991)
- Stanford Tau Beta Pi Award for Excellence in Undergraduate Teaching, Tau Beta Pi (1992)
- Best Paper Awards, IEDM (1993, 1995)
- Best Teacher Award, Society of Women Engineers (1995)
- Best Paper Award, ISPSD (1996)
- Elected Member, National Academy of Engineering (1996)
- Best Paper Award, MRS (2000)
- Best Paper Award, ICDS (2000)
- Third Millennium Medal, IEEE (2000)
- University Research Award, Semiconductor Industry Association (2001)
- Aldert Van der Ziel Award, IEEE (2003)
- J.J. Ebers Award, IEEE (2003)
- Laurels Award - Electronics, Aviation Week & Space Technology (2003)
- Jacob Millman Award, McGraw-Hill (2004)
- Paul Rappaport Award, IEDM (2006)

- UCLA Engineering Academic Alumnus of the Year, UCLA (2006)
- Andrew S. Grove Award, IEEE (2007)
- Elected Member, American Academy of Arts & Sciences (2008)
- Elected to Silicon Valley Engineering Hall of Fame, Silicon Valley Engineering Council (2014)
- IEEE Founders Medal, IEEE (2015)
- Elected to ISPSD Hall of Fame, International Symposium on Power Semiconductor Devices (2018)

## **BOARDS, ADVISORY COMMITTEES, PROFESSIONAL ORGANIZATIONS**

- Board of Trustees, Olin College of Engineering (2015 - present)
- Board of Directors, Cadence Corp (2011 - present)
- Board of Directors, Intel Corp (2005 - 2017)
- Board of Directors, Leadis Corp (2001 - 2010)
- Board of Directors, International Rectifier Corp (1995 - 2015)

## **PROGRAM AFFILIATIONS**

- Stanford SystemX Alliance

## **PROFESSIONAL EDUCATION**

- PhD, Stanford , Electrical Engineering (1971)
- MS, Stanford , Electrical Engineering (1967)
- BS, UCLA , Electrical Engineering (1966)

## **Research & Scholarship**

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### **CURRENT RESEARCH AND SCHOLARLY INTERESTS**

Dr. Plummer's early work focused on high voltage ICs and on high voltage device structures. He and his group made important contributions to integrating CMOS logic and high voltage lateral DMOS devices on the same chip and demonstrated circuits operating at several hundred volts. This work also led to several power MOS device concepts such as the IGBT which have become important power switching devices.

Throughout the 1980s and 90s, a major focus of his work was on silicon process modeling. This work involved many students and other faculty, particularly Professor Bob Dutton, and resulted in the development of several generations of SUPREM, which has become the standard process modeling tool used worldwide today. Dr. Plummer's contributions were principally in the areas of physical understanding and modeling of oxidation, diffusion, ion implantation and annealing. His recent work has focused on nanoscale silicon devices for logic and memory and has demonstrated new device concepts including vertical MOSFETs, the TRAM thyristor memory cell and the IMOS device which achieves  $< kT/q$  subthreshold slopes. Recent work has also focused on wide bandgap semiconductor materials, particularly SiC and GaN, for power control devices.

## **Teaching**

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### **COURSES**

#### **2022-23**

- Integrated Circuit Fabrication Processes: EE 212 (Aut)
- Power Semiconductor Devices and Technology: EE 218 (Spr)

#### **2021-22**

- Integrated Circuit Fabrication Processes: EE 212 (Aut)

#### 2020-21

- An Intro to Making: What is EE: ENGR 40M (Spr)
- Integrated Circuit Fabrication Processes: EE 212 (Aut)
- Power Semiconductor Devices and Technology: EE 218 (Win)

#### 2019-20

- An Intro to Making: What is EE: ENGR 40M (Spr)
- Integrated Circuit Fabrication Processes: EE 212 (Aut)
- Power Semiconductor Devices and Technology: EE 218 (Win)

## STANFORD ADVISEES

### Doctoral Dissertation Reader (AC)

Seungbin Jeong, Jia Zhuang

### Master's Program Advisor

Ottar Yngvason

## Publications

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### PUBLICATIONS

- **Rapid Melt Growth of Single Crystal InGaAs on Si Substrates** *ADVANCES IN MATERIALS SCIENCE AND ENGINEERING*  
Bai, X., Chen, C., Mukherjee, N., Griffin, P. B., Plummer, J. D.  
2016
- **Si incorporation from the seed into Ge stripes crystallized using rapid melt growth** *APPLIED PHYSICS LETTERS*  
Bai, X., Chen, C., Griffin, P. B., Plummer, J. D.  
2014; 104 (5)
- **Low-Temperature Monolithic Three-Layer 3-D Process for FPGA** *IEEE ELECTRON DEVICE LETTERS*  
Zhang, Z., Chen, C., Crnogorac, F., Chen, S., Griffin, P. B., Pease, R. F., Plummer, J. D., Wong, S. S.  
2013; 34 (8): 1044-1046
- **Low-Temperature Monolithic 3-Layer 3-D Process for FPGA** *IEEE Elec. Dev. Letters*  
Zhang, Z., Chen, C., Y., Crnogorac, F., Chen, S., L., Griffin, P., B., Pease, R., F., Plummer, J.  
2013; 34 (8): 1044-1046
- **Optimal Device Architecture and Hetero-Integration Scheme for III-V CMOS**  
Yuan, Z., Kumar, A., Chen, C., Y., Nainani, A., Griffin, P., Plummer, J.  
2013
- **Si Incorporation From the Seed Into Ge Stripes Crystallized Using Rapid Melt Growth** *submitted to APL*  
Bai, X., Chen, C., Y., Griffin, P., B., Plummer, J., D.  
2013
- **The Future of the Semiconductor Industry and What Does This Imply for Universities?**  
Plummer, J., D.  
2012
- **Statistical Retardation Delay of I-MOS and Its Measurement Using TDR** *IEEE ELECTRON DEVICE LETTERS*  
Cho, H., Onal, C., Griffin, P. B., Plummer, J. D.  
2011; 32 (2): 206-208

- **A High-Resolution Low-Power Incremental Sigma Delta ADC With Extended Range for Biosensor Arrays** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*  
Agah, A., Vleugels, K., Griffin, P. B., Ronaghi, M., Plummer, J. D., Wooley, B. A.  
2010; 45 (6): 1099-1110
- **Single-Crystal GaAs and GaSb on Insulator on Bulk Si Substrates Based on Rapid Melt Growth** *IEEE ELECTRON DEVICE LETTERS*  
Chen, S., Griffin, P. B., Plummer, J. D.  
2010; 31 (6): 597-599
- **High Quality Single-Crystal Laterally Graded SiGe on Insulator by Rapid Melt Growth** *ELECTROCHEMICAL AND SOLID STATE LETTERS*  
Koh, H. S., Chen, S., Griffin, P. B., Plummer, J. D.  
2010; 13 (8): H281-H283
- **Si CMOS – What happens When Scaling Isn’t An Option?**  
Plummer, J., D.  
2010
- **High-Resolution Low-Power Incremental ADC With Extended Range for Biosensor Arrays** *IEEE Journal of Solid State Circuits*  
Agah, A., Vleugels, K., Griffin, P. B., Ronaghi, M., Plummer, J. D., Wooley, B. A.  
2010; 45 (6): 1099-1110
- **High-quality single-crystal laterally graded SiGe on insulator by rapid melt growth** *Electrochem. Soc. Solid-State Lett*  
Koh, H., Y. Serene, Chen, S., Griffin, Peter, B., Plummer, James, D.  
2010; 13 (8): 281-283
- **Second generation monolithic full-depletion radiation sensor with integrated CMOS circuitry** *IEEE Nuclear Science Symposium (NSS)/Medical Imaging Conference (MIC)/17th International Workshop on Room-Temperature Semiconductor X-ray and Gamma-ray Detectors*  
Segal, J. D., Kenney, C. J., Parker, S. I., Aw, C. H., Snoeys, W. J., Wooley, B., Plummer, J. D.  
IEEE.2010: 1896–1900
- **Negative Differential Resistance Circuit Design and Memory Applications** *IEEE TRANSACTIONS ON ELECTRON DEVICES*  
Chen, S., Griffin, P. B., Plummer, J. D.  
2009; 56 (4): 634-640
- **A Novel Depletion-IMOS (DIMOS) Device With Improved Reliability and Reduced Operating Voltage** *IEEE ELECTRON DEVICE LETTERS*  
Onal, C., Woo, R., Koh, H. S., Griffin, P. B., Plummer, J. D.  
2009; 30 (1): 64-67
- **High-performance gate-all-around GeOI p-MOSFETs fabricated by rapid melt growth using plasma nitridation and ALD Al<sub>2</sub>O<sub>3</sub> gate dielectric and self-aligned NiGe contacts** *IEEE ELECTRON DEVICE LETTERS*  
Feng, J., Thareja, G., Kobayashi, M., Chen, S., Poon, A., Bai, Y., Griffin, P. B., Wong, S. S., Nishi, Y., Plummer, J. D.  
2008; 29 (7): 805-807
- **Opportunities and Challenges in the Semiconductor Industry**  
Plummer, J., D.  
2008
- **BTBT Transistor Scaling: Can they be Competitive with MOSFETs? 2008 DRC**  
Woo, R., Koh, H., Y. Serene, Onal, C., Griffin, P. B., Plummer, James, D.  
2008
- **P-channel germanium FinFET based on rapid melt growth** *IEEE ELECTRON DEVICE LETTERS*  
Feng, J., Woo, R., Chen, S., Liu, Y., Griffin, P. B., Plummer, J. D.  
2007; 28 (7): 637-639
- **Mechanism of solid phase crystallization of prepatterned nanoscale alpha-Si pillars** *JOURNAL OF APPLIED PHYSICS*  
Cho, H., Greene, B. J., Hoyt, J. L., Plummer, J. D.  
2007; 101 (10)
- **Modeling of surrounding gate MOSFETs with bulk trap states** *IEEE TRANSACTIONS ON ELECTRON DEVICES*  
Cho, H., Plummer, J. D.

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2007; 54 (1): 166-169

- **A High-Resolution Low-Power Oversampling ADC with Extended-Range for Bio-Sensor Arrays**  
Agah, A., Vleugels, K., Griffin, P. B., Ronaghi, M., Plummer, J. D., Wooley, B. A.  
2007
- **A high-resolution low-power oversampling ADC with extended-range for bio-sensor Arrays** *20th Symposium on VLSI Circuits*  
Agah, A., Vleugels, K., Griffin, P. B., Rodaghi, M., Plummer, J. D., Wooley, B. A.  
JAPAN SOCIETY APPLIED PHYSICS.2007: 244–245
- **Monolithic 3D integrated circuits** *International Symposium on VLSI Technology, Systems and Applications*  
Wong, S., El-Gamal, A., Griffin, P., Nishi, Y., Pease, F., Plummer, J.  
IEEE.2007: 66–69
- **A semiclassical model of dielectric relaxation in glasses** *JOURNAL OF APPLIED PHYSICS*  
Jameson, J. R., Harrison, W., Griffin, P. B., Plummer, J. D., Nishi, Y.  
2006; 100 (12)
- **Integration of germanium-on-insulator and silicon MOSFETs on a silicon substrate** *IEEE ELECTRON DEVICE LETTERS*  
Feng, J., Liu, Y., Griffin, P. B., Plummer, J. D.  
2006; 27 (11): 911-913
- **Charge trapping in high-k gate stacks due to the bilayer structure itself** *IEEE TRANSACTIONS ON ELECTRON DEVICES*  
Jameson, J. R., Griffin, P. B., Plummer, J. D., Nishi, Y.  
2006; 53 (8): 1858-1867
- **Novel Methods for Ultrashallow Low Resistance Junction Formation**  
Jain, S., Griffin, P., B., Plummer, J., D.  
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- **Novel Methods for Ultrashallow Low Resistance Junction Formation**  
Jain, S., H., Griffin, P., B., Plummer, J., D.  
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- **Novel Methods for Ultrashallow Low Resistance Junction Formation**  
Jain, S., Griffin, P., B., Plummer, J., D.  
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- **Low resistance, low-leakage ultrashallow p(+)-junction formation using millisecond flash anneals** *IEEE TRANSACTIONS ON ELECTRON DEVICES*  
Jain, S. H., Griffin, P. B., Plummer, J. D., McCoy, S., Gelpey, J., Selinger, T., Downey, D. F.  
2005; 52 (7): 1610-1615
- **Novel very high IE structures based on the directed BBHE mechanism for ultralow-power flash memories** *IEEE ELECTRON DEVICE LETTERS*  
Gopalakrishnan, K., Woo, R., Shenoy, R., Jono, Y., Griffin, P. B., Plummer, J. D.  
2005; 26 (3): 212-215
- **Critical thickness enhancement of epitaxial SiGe films grown on small structures** *JOURNAL OF APPLIED PHYSICS*  
Liang, Y., Nix, W. D., Griffin, P. B., Plummer, J. D.  
2005; 97 (4)
- **Impact ionization MOS (I-MOS) - Part I: Device and circuit simulations** *IEEE TRANSACTIONS ON ELECTRON DEVICES*  
Gopalakrishnan, K., Griffin, P. B., Plummer, J. D.  
2005; 52 (1): 69-76
- **Ni<sub>2</sub>Si and NiSi formation by low temperature soak and spike RTPs** *13th IEEE International Conference on Advanced Thermal Processing of Semiconductor*  
Kim, E. H., Forstner, H., Foad, M., Tam, N., Ramamurthy, S., Griffin, P. B., Plummer, J. D.  
IEEE.2005: 177–181
- **Ni<sub>2</sub> and NiSi Formation by Low Temperature Soak and Spike RTPs**  
Kim, E., Forstner, H., Foad, M., Tam, N., Ramamurthy, S., Griffin, P., B., Plummer, J.

2005

- **A Novel SiGe-based Negative Differential Resistance (NDR) Device**  
Liang, Y., Gopalakrishnan, K., Griffin, P. B., Plummer, J. D.  
2005
- **From DRAM to SRAM with a novel SiGe-based negative differential resistance (NDR) device** *IEEE International Electron Devices Meeting*  
Liang, Y., Gopalakrishnan, K., Griffin, P. B., Plummer, J. D.  
IEEE.2005: 979–982
- **Design requirements for integrated biosensor arrays** *Conference on Imaging, Manipulation, and Analysis of Biomolecules and Cells - Fundamentals and Applications III*  
Agah, A., Hassibi, A., Plummer, J. D., Griffin, P. B.  
SPIE-INT SOC OPTICAL ENGINEERING.2005: 403–413
- **Rapid melt growth of germanium crystals with self-aligned microcrucibles on Si substrates** *JOURNAL OF THE ELECTROCHEMICAL SOCIETY*  
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2005; 152 (8): G688-G693
- **Impact ionization MOS (I-MOS) - Part II: Experimental results** *IEEE TRANSACTIONS ON ELECTRON DEVICES*  
Gopalakrishnan, K., Woo, R., Jungemann, C., Griffin, P. B., Plummer, J. D.  
2005; 52 (1): 77-84
- **Metastable boron active concentrations in Si using flash assisted solid phase epitaxy** *JOURNAL OF APPLIED PHYSICS*  
Jain, S. H., Griffin, P. B., Plummer, J. D., McCoy, S., Gelpey, J., Selinger, T., Downey, D. F.  
2004; 96 (12): 7357-7360
- **Double-well model of dielectric relaxation current** *APPLIED PHYSICS LETTERS*  
Jameson, J. R., Harrison, W., Griffin, P. B., Plummer, J. D.  
2004; 84 (18): 3489-3491
- **Diffuse x-ray scattering and transmission electron microscopy study of defects in antimony-implanted silicon** *JOURNAL OF APPLIED PHYSICS*  
Takamura, Y., Marshall, A. F., Mehta, A., ARTHUR, J., Griffin, P. B., Plummer, J. D., Patel, J. R.  
2004; 95 (8): 3968-3976
- **High-quality single-crystal Ge on insulator by liquid-phase epitaxy on Si substrates** *APPLIED PHYSICS LETTERS*  
Liu, Y. C., Deal, M. D., Plummer, J. D.  
2004; 84 (14): 2563-2565
- **Carrier profiling via scanning tunneling spectroscopy: Comparison with scanning capacitance microscopy** *7th International Workshop on the Fabrication, Characterization and Modeling of Ultra-Shallow Doping Profiles in Semiconductors*  
Liu, F. Y., Griffin, P. B., Plummer, J. D., Lyding, J. W., Moran, J. M., Richards, J. F., Kulig, L.  
A V S AMER INST PHYSICS.2004: 422–26
- **High Quality Single-crystal Ge-on-insulator by Liquid-phase Epitaxy on Si Substrates** *Appl. Phys. Letters*  
Liu, Y., Deal, M., D., Plummer, J., D.  
2004; 84 (14): 2563–2565
- **What's Hot in Engineering – A Look at the Next 25 years**  
Plummer, J., D.  
2004
- **Silicon-based Devices and Technology for the Nanoscale Era**  
Plummer, J., D.  
2004
- **Low Resistant Contacts to Laser Annealed Junctions**  
Kim, E., Griffin, P., B., Plummer, J., D.  
2004
- **Critical Thickness Enhancement of Epitaxial SiGe Films Grown on Small Structures**

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- Liang, Y., Nix, W., D., Griffin, P., B., Plummer, J., D.  
2004
- **CMOS Compatible Liquid-Phase Epitaxial Growth of Ge on Si Substrates**  
Liu, Y., Deal, M., D., Plummer, J., D.  
2004
  - **Metastable Active Concentrations in Si Using Flash Assisted Solid Phase Epitaxy** *J. Appl. Phys.*  
Jain, S., H., Griffin, P., B., Plummer, J., D., McCoy, S., Gelpey, J., Selinger, T.  
2004; 96 (12): 7357-7360
  - **MOSFETs and high-speed photodetectors on Ge-on-insulator substrates fabricated using rapid melt growth** *50th IEEE International Electron Devices Meeting*  
Liu, Y. C., Gopalakrishnan, K., Griffin, P. B., Ma, K., Deal, M. D., Plummer, J. D.  
IEEE.2004: 1001-1004
  - **A multi-enzyme model for pyrosequencing** *NUCLEIC ACIDS RESEARCH*  
Agah, A., Aghajan, M., Mashayekhi, F., Amini, S., Davis, R. W., Plummer, J. D., Ronaghi, M., Griffin, P. B.  
2004; 32 (21)
  - **Atomistic modeling of deactivation and reactivation mechanisms in high-concentration boron profiles** *APPLIED PHYSICS LETTERS*  
Aboy, M., Pelaz, L., Marques, L. A., Barbolla, J., Mokhberi, A., Takamura, Y., Griffin, P. B., Plummer, J. D.  
2003; 83 (20): 4166-4168
  - **Activation and diffusion studies of ion-implanted p and n dopants in germanium** *APPLIED PHYSICS LETTERS*  
Chui, C. O., Gopalakrishnan, K., Griffin, P. B., Plummer, J. D., Saraswat, K. C.  
2003; 83 (16): 3275-3277
  - **Hall measurements of bilayer structures** *JOURNAL OF APPLIED PHYSICS*  
Jain, S. H., Griffin, P. B., Plummer, J. D.  
2003; 93 (2): 1060-1063
  - **Atomistic modeling of B activation and deactivation for ultra-shallow junction formation** *IEEE International Conference on Simulation of Semiconductor Processes and Devices*  
Aboy, M., Pelaz, L., Marques, L. A., Barbolla, J., Mokhberi, A., Takamura, Y., Griffin, P. B., Plummer, J. D.  
IEEE.2003: 151-154
  - **Carrier Profiling via STM/STS; Comparison with SCM and SIMS**  
Liu, F., Y., Griffin, P., B., Plummer, J., D., Lyding, J., W, Morse, J., M., Richards, J., F.  
2003
  - **School of Engineering Strategic Initiatives** *E-DAY Keynote*  
Plummer, J., D.  
2003
  - **Stress effects on nanocrystal formation by Ni-induced crystallization of amorphous Si** *Symposium on Amorphous and Nanocrystalline Silicon-Based Films held at the 2003 MRS Spring Meeting*  
Liu, Y. C., Deal, M. D., Sultana, M., Plummer, J. D.  
MATERIALS RESEARCH SOCIETY.2003: 669-673
  - **Problems with metal-oxide high-K dielectrics due to 1/t dielectric relaxation current in amorphous materials** *IEEE International Electron Devices Meeting*  
Jameson, J. R., Griffin, P. B., Agah, A., Plummer, J. D., Kim, H. S., Taylor, D. V., McIntyre, P. C., Harrison, W. A.  
IEEE.2003: 91-94
  - **The use of laser annealing to reduce parasitic series resistances in MOS devices** *14th International Conference on Ion Implantation Technology*  
Takamura, Y., Kim, E. H., Jain, S. H., Griffin, P. B., Plummer, J. D.  
IEEE.2003: 56-59
  - **Single-crystalline Si on insulator in confined structures fabricated by two-step metal-induced crystallization of amorphous Si** *APPLIED PHYSICS LETTERS*  
Liu, Y. C., Deal, M. D., Saraswat, K. C., Plummer, J. D.



2002; 81 (24): 4634-4636

- **Impact of lateral source/drain abruptness on device performance** *IEEE TRANSACTIONS ON ELECTRON DEVICES*  
Kwong, M. Y., Kasnavi, R., Griffin, P., Plummer, J. D., DUTTON, R. W.  
2002; 49 (11): 1882-1890
- **Dopant deactivation in heavily Sb doped Si (001): A high-resolution x-ray diffraction and transmission electron microscopy study** *JOURNAL OF APPLIED PHYSICS*  
Takamura, Y., Vailionis, A., Marshall, A. F., Griffin, P. B., Plummer, J. D.  
2002; 92 (9): 5503-5507
- **Silicon orientation effects in the initial regime of wet oxidation** *JOURNAL OF THE ELECTROCHEMICAL SOCIETY*  
Ngau, J. L., Griffin, P. B., Plummer, J. D.  
2002; 149 (8): F98-F101
- **Physical processes associated with the deactivation of dopants in laser annealed silicon** *JOURNAL OF APPLIED PHYSICS*  
Takamura, Y., Griffin, P. B., Plummer, J. D.  
2002; 92 (1): 235-244
- **A comparative study of dopant activation in boron, BF<sub>2</sub>, arsenic, and phosphorus implanted silicon** *IEEE TRANSACTIONS ON ELECTRON DEVICES*  
Mokhberi, A., Griffin, P. B., Plummer, J. D., Paton, E., McCoy, S., Elliott, K.  
2002; 49 (7): 1183-1191
- **Thermal stability of dopants in laser annealed silicon** *JOURNAL OF APPLIED PHYSICS*  
Takamura, Y., Jain, S. H., Griffin, P. B., Plummer, J. D.  
2002; 92 (1): 230-234
- **Fluorine interaction with point defects, boron, and arsenic in ion-implanted Si** *APPLIED PHYSICS LETTERS*  
Mokhberi, A., Kasnavi, R., Griffin, P. B., Plummer, J. D.  
2002; 80 (19): 3530-3532
- **Atomic-scale diffusion mechanisms via intermediate species** *PHYSICAL REVIEW B*  
Ural, A., Griffin, P. B., Plummer, J. D.  
2002; 65 (13)
- **A physics based approach to ultra-shallow p(+) -junction formation at the 32nm node** *IEEE International Electron Devices Meeting*  
Mokhberi, A., Pelaz, L., Aboy, M., Marves, L., Barbolla, J., Paton, E., McCoy, S., Ross, J., Elliott, K., Gelpey, J., Griffin, P. B., Plummer, J. D.  
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- **Thermal Stability of Laser Annealed Dopants in Silicon** *J. Appl. Physics*  
Takamura, Y., Jain, S., Griffin, P., B., Plummer, J., D.  
2002; 92: 230
- **Miniaturized DNA Analysis Devices**  
Griffin, P., Agah, A., Plummer, J., D., Eltoukhy, P., H., Salama, K., Gamal, A., El  
2002
- **Dopant Deactivation in Heavily Sb Doped Si (001): High Resolution X-ray Diffraction Study**  
Takamura, Y., Vailionis, A., Griffin, P., B., Plummer, J., D.  
2002
- **A Study of the Deactivation of High Concentration, Laser Annealed Dopant Profiles in Silicon**  
Ngau, J., L., Griffin, P., B., Plummer, J., D.  
2002
- **The local structure of antimony in high dose antimony implants in silicon by XAFS and SIMS** *Symposium on Silicon Front-End Junction Formation Technologies held at the MRS Spring Meeting*  
Sahiner, M. A., Novak, S. W., Woicik, J. C., Takamura, Y., Griffin, P. B., Plummer, J. D.  
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- **I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q** *IEEE International Electron Devices Meeting*

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- Gopalakrishnan, K., Griffin, P. B., Plummer, J. D.  
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