

# Stanford

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## David Dill

Donald E. Knuth Professor in the School of Engineering, Emeritus  
Computer Science

### CONTACT INFORMATION

- **Administrator**

Mary Jane Swenson - Administrative Associate

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### Bio

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#### BIO

Dill has interests in computational systems biology as well as the theory and application of formal verification techniques to system designs, which encompass hardware, protocols, and software. He has also done research in asynchronous circuit verification and synthesis, and in verification methods for hard real-time systems.

#### ACADEMIC APPOINTMENTS

- Professor Emeritus, Computer Science
- Member, Bio-X

#### HONORS AND AWARDS

- Pioneer Award, Electronic Frontier Foundation
- Fellow, IEEE
- Fellow, ACM
- Member, National Academy of Engineering (2013)
- Fellow, American Academy of Arts and Sciences (2013)

#### PROFESSIONAL EDUCATION

- PhD, Carnegie Mellon (1987)

#### LINKS

- <http://verify.stanford.edu/dill>: <http://verify.stanford.edu/dill>

### Research & Scholarship

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#### CURRENT RESEARCH AND SCHOLARLY INTERESTS

Computational methods for understanding regulatory circuits in cell biology

## Teaching

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### COURSES

#### 2016-17

- Departmental Lecture Series: CS 300 (Aut)

#### 2015-16

- Advanced Topics in Formal Methods: CS 357 (Aut)
- Departmental Lecture Series: CS 300 (Aut)

#### 2014-15

- Compilers: CS 143 (Spr)
- Departmental Lecture Series: CS 300 (Aut)
- Elections and Technology: CS 76N (Aut)
- Mathematical Foundations of Computing: CS 103 (Win)

### GRADUATE AND FELLOWSHIP PROGRAM AFFILIATIONS

- Biomedical Informatics (Phd Program)

## Publications

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### PUBLICATIONS

- **Systematic discovery of mutation-specific synthetic lethals by mining pan-cancer human primary tumor data.** *Nature communications*  
Sinha, S., Thomas, D., Chan, S., Gao, Y., Brunen, D., Torabi, D., Reinisch, A., Hernandez, D., Chan, A., Rankin, E. B., Bernards, R., Majeti, R., Dill, et al  
2017; 8: 15580-?
- **Cell cycle progression in *Caulobacter* requires a nucleoid-associated protein with high AT sequence recognition** *PROCEEDINGS OF THE NATIONAL ACADEMY OF SCIENCES OF THE UNITED STATES OF AMERICA*  
Ricci, D. P., Melfi, M. D., Lasker, K., Dill, D. L., McAdams, H. H., Shapiro, L.  
2016; 113 (40): E5952-E5961
- **A Pharmacogenetic Discovery: Cystamine Protects Against Haloperidol-Induced Toxicity and Ischemic Brain Injury** *GENETICS*  
Zhang, H., Zheng, M., Wu, M., Xu, D., Nishimura, T., Nishimura, Y., Giffard, R., Xiong, X., Xu, L. J., Clark, J. D., Sahbaie, P., Dill, D. L., Peltz, et al  
2016; 203 (1): 599-?
- **The multiple PDZ domain protein Mpdz/MUPP1 regulates opioid tolerance and opioid-induced hyperalgesia** *BMC GENOMICS*  
Donaldson, R., Sun, Y., Liang, D., Zheng, M., Sahbaie, P., Dill, D. L., Peltz, G., Buck, K. J., Clark, J. D.  
2016; 17
- **CauloBrowser: A systems biology resource for *Caulobacter crescentus*.** *Nucleic acids research*  
Lasker, K., Schrader, J. M., Men, Y., Marshik, T., Dill, D. L., McAdams, H. H., Shapiro, L.  
2016; 44 (D1): D640-5
- **CauloBrowser: A systems biology resource for *Caulobacter crescentus*.** *Nucleic acids research*  
Lasker, K., Schrader, J. M., Men, Y., Marshik, T., Dill, D. L., McAdams, H. H., Shapiro, L.  
2016; 44 (D1): D640-5
- **Towards in vivo estimation of reaction kinetics using high-throughput metabolomics data: a maximum likelihood approach** *BMC SYSTEMS BIOLOGY*  
Zhang, W., Kolte, R., Dill, D. L.  
2015; 9
- **The role of Abcb5 alleles in susceptibility to haloperidol-induced toxicity in mice and humans.** *PLoS medicine*  
Zheng, M., Zhang, H., Dill, D. L., Clark, J. D., Tu, S., Yablonovitch, A. L., Tan, M. H., Zhang, R., Rujescu, D., Wu, M., Tessarollo, L., Vieira, W., Gottesman, et al

2015; 12 (2)

- **The role of *abcb5* alleles in susceptibility to haloperidol-induced toxicity in mice and humans.** *PLoS medicine*  
Zheng, M., Zhang, H., Dill, D. L., Clark, J. D., Tu, S., Yablonovitch, A. L., Tan, M. H., Zhang, R., Rujescu, D., Wu, M., Tessarollo, L., Vieira, W., Gottesman, et al  
2015; 12 (2)
- **Mutant WT1 is associated with DNA hypermethylation of PRC2 targets in AML and responds to EZH2 inhibition.** *Blood*  
Sinha, S., Thomas, D., Yu, L., Gentles, A. J., Jung, N., Corces-Zimmerman, M. R., Chan, S. M., Reinisch, A., Feinberg, A. P., Dill, D. L., Majeti, R.  
2015; 125 (2): 316-326
- **The global regulatory architecture of transcription during the *Caulobacter* cell cycle.** *PLoS genetics*  
Zhou, B., Schrader, J. M., Kalogeraki, V. S., Abeliuk, E., Dinh, C. B., Pham, J. Q., Cui, Z. Z., Dill, D. L., McAdams, H. H., Shapiro, L.  
2015; 11 (1)
- **The Global Regulatory Architecture of Transcription during the *Caulobacter* Cell Cycle.** *PLoS genetics*  
Zhou, B., Schrader, J. M., Kalogeraki, V. S., Abeliuk, E., Dinh, C. B., Pham, J. Q., Cui, Z. Z., Dill, D. L., McAdams, H. H., Shapiro, L.  
2015; 11 (1)
- **Towards in vivo estimation of reaction kinetics using high-throughput metabolomics data: a maximum likelihood approach.** *BMC systems biology*  
Zhang, W., Kolte, R., Dill, D. L.  
2015; 9: 66-?
- **MYC through miR-17-92 Suppresses Specific Target Genes to Maintain Survival, Autonomous Proliferation, and a Neoplastic State.** *Cancer cell*  
Li, Y., Choi, P. S., Casey, S. C., Dill, D. L., Felsher, D. W.  
2014; 26 (2): 262-272
- **Automated identification of stratifying signatures in cellular subpopulations** *PROCEEDINGS OF THE NATIONAL ACADEMY OF SCIENCES OF THE UNITED STATES OF AMERICA*  
Bruggner, R. V., Bodenmiller, B., Dill, D. L., Tibshirani, R. J., Nolan, G. P.  
2014; 111 (26): E2770-E2777
- **Automated identification of stratifying signatures in cellular subpopulations.** *Proceedings of the National Academy of Sciences of the United States of America*  
Bruggner, R. V., Bodenmiller, B., Dill, D. L., Tibshirani, R. J., Nolan, G. P.  
2014; 111 (26): E2770-7
- **Mining TCGA data using Boolean implications.** *PloS one*  
Sinha, S., Tsang, E. K., Zeng, H., Meister, M., Dill, D. L.  
2014; 9 (7)
- **Mining TCGA Data Using Boolean Implications.** *PloS one*  
Sinha, S., Tsang, E. K., Zeng, H., Meister, M., Dill, D. L.  
2014; 9 (7)
- **Liquid chromatography/mass spectrometry methods for measuring dipeptide abundance in non-small-cell lung cancer.** *Rapid communications in mass spectrometry : RCM*  
Wu, M., Xu, Y., Fitch, W. L., Zheng, M., Merritt, R. E., Shrager, J. B., Zhang, W., Dill, D. L., Peltz, G., Hoang, C. D.  
2013; 27 (18): 2091-2098
- **Identification of drug targets by chemogenomic and metabolomic profiling in yeast** *PHARMACOGENETICS AND GENOMICS*  
Wu, M., Zheng, M., Zhang, W., Suresh, S., Schlecht, U., Fitch, W. L., Aronova, S., Baumann, S., Davis, R., St Onge, R., Dill, D. L., Peltz, G.  
2012; 22 (12): 877-886
- **Computational genetic discoveries that could improve perioperative medicine** *CURRENT OPINION IN ANESTHESIOLOGY*  
Zheng, M., Dill, D., Clark, J. D., Peltz, G.  
2012; 25 (4): 428-433
- **Gene Expression Commons: An Open Platform for Absolute Gene Expression Profiling** *PLOS ONE*  
Seita, J., Sahoo, D., Rossi, D. J., Bhattacharya, D., Serwold, T., Inlay, M. A., Ehrlich, L. I., Fathman, J. W., Dill, D. L., Weissman, I. L.  
2012; 7 (7)
- **Cd14 SNPs regulate the innate immune response** *MOLECULAR IMMUNOLOGY*

- Liu, H., Hu, Y., Zheng, M., Suhoski, M. M., Engleman, E. G., Dill, D. L., Hudnall, M., Wang, J., Spolski, R., Leonard, W. J., Peltz, G.  
2012; 51 (2): 112-127
- **A better prognosis for genetic association studies in mice** *TRENDS IN GENETICS*  
Zheng, M., Dill, D., Peltz, G.  
2012; 28 (2): 62-69
  - **Cd14 SNPs regulate the innate immune response** *Molecular Immunology*  
Lu, H., Hu, Y., Zheng, M., Engleman, E., Dill, D., Hudnall, M.  
2012; 2 (51): 112-127
  - **Computational genetic discoveries that could improve perioperative medicine** *Current Opinion in Anesthesiology*  
Zheng, M., Dill, D., Clark, J., Peltz, G.  
2012
  - **Gene Expression Commons: an open platform for absolute gene expression profiling** *PLoS One*  
Seita, J., Sahoo, D., Rossi, D., Bhattacharya, D., Serwold, T., Inlay, M., Dill, D.  
2012; 7
  - **A better prognosis for genetic association studies in mice** *Trends in Genetics*  
Zheng, M., Dill, D., Peltz, G.  
2012; 2 (28): 62-69
  - **Identification of drug targets by chemogenomic and metabolomic profiling in yeast.** *Pharmacogenetic Genomics*  
Wu, M., Zheng, M., Zhang, W., Suresh, S., Schlecht, U., Fitch, W. L., Dill, D.  
2012
  - **Next-Generation Computational Genetic Analysis: Multiple Complement Alleles Control Survival after Candida albicans Infection** *INFECTION AND IMMUNITY*  
Peltz, G., Zaas, A. K., Zheng, M., Solis, N. V., Zhang, M. X., Liu, H., Hu, Y., Boxx, G. M., Phan, Q. T., Dill, D., Filler, S. G.  
2011; 79 (11): 4472-4479
  - **Are Cells Asynchronous Circuits? (Invited Talk)** *12th International Conference on Verification, Model Checking, and Abstract Interpretation*  
Dill, D. L.  
SPRINGER-VERLAG BERLIN.2011: 1-1
  - **Next-generation computational genetic analysis: Multiple complement alleles control survival after candida albicans infection** *Infection and Immunity*  
Peltz, G., Zaas, A., K., Zheng, M., Solis, N., V., Zhang, M., X., Liu, H., H., Dill, D.  
2011; 11 (79): 4472-4479
  - **The Role of Interleukin-1 in Wound Biology. Part II: In Vivo and Human Translational Studies** *ANESTHESIA AND ANALGESIA*  
Hu, Y., Liang, D., Li, X., Liu, H., Zhang, X., Zheng, M., Dill, D., Shi, X., Qiao, Y., Yeomans, D., Carvalho, B., Angst, M. S., Clark, et al  
2010; 111 (6): 1534-1542
  - **The Role of Interleukin-1 in Wound Biology. Part I: Murine In Silico and In Vitro Experimental Analysis** *ANESTHESIA AND ANALGESIA*  
Hu, Y., Liang, D., Li, X., Liu, H., Zhang, X., Zheng, M., Dill, D., Shi, X., Qiao, Y., Yeomans, D., Carvalho, B., Angst, M. S., Clark, et al  
2010; 111 (6): 1525-1533
  - **MiDReG: A method of mining developmentally regulated genes using Boolean implications** *PROCEEDINGS OF THE NATIONAL ACADEMY OF SCIENCES OF THE UNITED STATES OF AMERICA*  
Sahoo, D., Seita, J., Bhattacharya, D., Inlay, M. A., Weissman, I. L., Plevritis, S. K., Dill, D. L.  
2010; 107 (13): 5732-5737
  - **Timing Robustness in the Budding and Fission Yeast Cell Cycles** *PLOS ONE*  
Mangla, K., Dill, D. L., Horowitz, M. A.  
2010; 5 (2)
  - **The role of interleukin-1 in wound biology. part i: murine in silico and in vitro experimental analysis** *Anesthesia & Analgesia*  
Hu, Y., Liang, D., Li, X., Liu, H., Zhang, X., Zheng, M., Dill, D.  
2010; 6 (111): 1525-1533

- **Timing robustness in the budding and fission yeast cell cycles** *PLoS ONE*  
Mangla, K., Dill, D. L., Horowitz, M. A.  
2010; 2 (5): e8906
- **The role of interleukin-1 in wound biology. part ii: in vivo and human translational studies** *Anesthesia & nalgesia*  
Hu, Y., Liang, D., Li, X., Liu, H., Zhang, X., Zheng, M., Dill, D.  
2010; 6 (111): 1534–1542
- **Gene expression changes induced by genistein in the prostate cancer cell line Incap** *Open Prostate Cancer J*  
Bhamre, S., Sahoo, D., Tibshirani, R., Dill, D. L., Brooks, J., D  
2010; 3: 86–98
- **Ly6d marks the earliest stage of B-cell specification and identifies the branchpoint between B-cell and T-cell development** *GENES & DEVELOPMENT*  
Inlay, M. A., Bhattacharya, D., Sahoo, D., Serwold, T., Seita, J., Karsunky, H., Plevritis, S. K., Dill, D. L., Weissman, I. L.  
2009; 23 (20): 2376–2381
- **Temporal Changes in Gene Expression Induced by Sulforaphane in Human Prostate Cancer Cells** *PROSTATE*  
Bhamre, S., Sahoo, D., Tibshirani, R., Dill, D. L., Brooks, J. D.  
2009; 69 (2): 181–190
- **Temporal changes in gene expression induced by sulforaphane in human prostate cancer cells** *The Prostate*  
Bhamre, S., Sahoo, D., Tibshirani, R., Dill, D., Brooks, J.  
2009; 2 (69): 181–90
- **Ly6d marks the earliest stage of b-cell specification and identifies the branchpoint between b-cell and t-cell development** *Genes and Development*  
Inlay, Matthew, A., Bhattacharya, D., Sahoo, D., Serwold, T., Seita, J., Karsunky, H., Dill, D.  
2009; 20 (23): 2376–2381
- **EXE: Automatically Generating Inputs of Death** *13th ACM Conference on Computer and Communications Security*  
Cadair, C., Ganesh, V., Pawlowski, P. M., Dill, D. L., Engler, D. R.  
ASSOC COMPUTING MACHINERY.2008
- **Point/Counterpoint The U. S. Should Ban Paperless Electronic Voting Machines** *COMMUNICATIONS OF THE ACM*  
Dill, D. L.  
2008; 51 (10): 29–30
- **Architecture and inherent robustness of a bacterial cell-cycle control system** *PROCEEDINGS OF THE NATIONAL ACADEMY OF SCIENCES OF THE UNITED STATES OF AMERICA*  
Shen, X., Collier, J., Dill, D., Shapiro, L., Horowitz, M., McAdams, H. H.  
2008; 105 (32): 11340–11345
- **Genomic and proteomic analysis reveals a threshold level of MYC required for tumor maintenance** *CANCER RESEARCH*  
Shachaf, C. M., Gentles, A. J., Elchuri, S., Sahoo, D., Soen, Y., Sharpe, O., Perez, O. D., Chang, M., Mitchel, D., Robinson, W. H., Dill, D., Nolan, G. P., Plevritis, et al  
2008; 68 (13): 5132–5142
- **Combined Analysis of Murine and Human Microarrays and ChIP Analysis Reveals Genes Associated with the Ability of MYC To Maintain Tumorigenesis** *PLOS GENETICS*  
Wu, C., Sahoo, D., Arvanitis, C., Bradon, N., Dill, D. L., Felsher, D. W.  
2008; 4 (6)
- **Boolean implication networks derived from large scale, whole genome microarray datasets** *GENOME BIOLOGY*  
Sahoo, D., Dill, D. L., Gentles, A. J., Tibshirani, R., Plevritis, S. K.  
2008; 9 (10)
- **Boolean implication networks derived from large scale, whole genome microarray datasets** *Genome Biology*  
Sahoo, D., Dill, D. L., Gentles, A., J., Tibshirani, R., Plevritis, S., K.  
2008; 10 (9): R157
- **Architecture and inherent robustness of a bacterial cell-cycle control system** *Proceedings of the National Academy of Sciences*

- 
- Shen, X., Collier, J., Dill, D., L., Shapiro, L., Horowitz, M., McAdams, H., H.  
2008; 32 (105): 11340–11345
- **EXE: automatically generating inputs of death.** *ACM Transactions on Information and System Security*  
Cadar, C., Ganesh, V., Pawlowski, Peter, M., Dill, David, L., Engler, Dawson, R.  
2008; 2 (12)
  - **Combined analysis of murine and human microarrays and chip analysis reveals genes associated with the ability of myc to maintain tumorigenesis.** *PLoS Genetics*  
Wu, C., H., Sahoo, D., Arvanitis, C., Bradon, N., Dill, D., L., Felsher, D., W.  
2008; 6 (4)
  - **Genomic and proteomic analysis reveals a threshold level of myc required for tumor maintenance** *Cancer Research*  
Shachaf, C., M., Gentles, A., J., Elchuri, S., Sahoo, D., Soen, Y., Sharpe, O., Dill, D.  
2008; 13 (68): 5132
  - **Automatic Formal Verification of Block Cipher Implementations** *8th International Conference on Formal Methods in Computer-Aided Design*  
Smith, E. W., Dill, D. L.  
IEEE.2008: 45–51
  - **A retrospective on Mur phi** *Symposium on 25 Years of Model Checking (25MC)*  
Dill, D. L.  
SPRINGER-VERLAG BERLIN.2008: 77–88
  - **Extracting binary signals from microarray time-course data** *NUCLEIC ACIDS RESEARCH*  
Sahoo, D., Dill, D. L., Tibshirani, R., Plevritis, S. K.  
2007; 35 (11): 3705–3712
  - **A decision procedure for bit-vectors and arrays** *19th International Conference on Computer Aided Verification*  
Ganesh, V., Dill, D. L.  
SPRINGER-VERLAG BERLIN.2007: 519–531
  - **A retrospective on mur#** *In 25 years of Model Checking, volume 4925 of Lecture Notes in Computer Science*  
Dill, David, L.  
2007: 1
  - **Extracting boolean signals from microarray time course data.** *Nucleic Acids Research*  
Sahoo, D., Dill, David, L., Tibshirani, R., Plevritis, Sylvia, K.  
2007; 11 (35): 3705–3712
  - **The Pathalyzer: A tool for analysis of signal transduction pathways** *Joint Annual Workshop on Systems Biology and on Regulatory Genomics*  
Dill, D. L., Knapp, M. A., Gage, P., Talcott, C., Laderoute, K., Lincoln, P.  
SPRINGER-VERLAG BERLIN.2007: 11–22
  - **A refinement method for validity checking of quantified first-order formulas in hardware verification** *6th International Conference on Formal Methods in Computer Aided Design*  
Abu-Haimed, H., Dill, D. L., Berezin, S.  
IEEE COMPUTER SOC.2006: 145–152
  - **Multiple representations of biological processes.** *Transactions on Computational Systems Biology*  
Talcott, C., Dill, David, L.  
2006: 221–245
  - **Multiple representations of biological processes** *4th International Conference on Computational Methods in Systems Biology*  
Talcott, C., Dill, D. L.  
SPRINGER-VERLAG BERLIN.2006: 221–245
  - **The pathway logic assistant**  
Talcott, C., Dill, David, L.  
2005

- **Evaluation of voting systems.** *Commun. ACM*  
Vora, P., L., Adida, B., Bucholz, R., Chaum, D., Dill, D., L., Jefferson, D.  
2004; 11 (47): 144
- **A partitioning methodology for BDD-based verification** *5th International Conference on Formal Methods in Computer-Aided Design (FMCAD)*  
Sahoo, D., Iyer, S., Jain, J., Stangier, C., Narayan, A., Dill, D. L., Emerson, E. A.  
SPRINGER-VERLAG BERLIN.2004: 399–413
- **A practical approach to partial functions in CVC Lite.**  
Barrett, C., Berezin, S., Shikanian, I., Chechik, M., Gurfinkel, A., Dill, David, L.  
2004
- **A partitioning methodology for bdd-based verification**  
Sahoo, D., Iyer, Subramanian, K., Jain, J., Stangier, C., Narayan, A., Dill, David, L.  
2004
- **Guest editors' introduction: E-voting security.** *IEEE Security and Privacy*  
Dill, David, L., Rubin, Aviel, D.  
2004; 1 (2)
- **A proof-producing boolean search engine.**  
Barrett, C., Berezin, S., Dill, David, L.  
2003
- **Using formal specifications for functional validation of hardware designs** *IEEE DESIGN & TEST OF COMPUTERS*  
Shimizu, K., Dill, D. L.  
2002; 19 (4): 96-106
- **Efficient algorithms for approximate time separation of events** *SADHANA-ACADEMY PROCEEDINGS IN ENGINEERING SCIENCES*  
Chakraborty, S., Dill, D. L., Yun, K. Y.  
2002; 27: 129-162
- **Formal verification of out-of-order execution with incremental flushing** *FORMAL METHODS IN SYSTEM DESIGN*  
Jones, R. B., Skakkebaek, J. U., Dill, D. L.  
2002; 20 (2): 139-158
- **Counter-example based predicate discovery in predicate abstraction** *4th International Conference on Formal Methods in Computer-Aided Design (FMCAD 2002)*  
Das, S., Dill, D. L.  
SPRINGER-VERLAG BERLIN.2002: 19–32
- **CVC: a Cooperating Validity Checker.**  
Stump, A., Barrett, C., Dill, D.  
2002
- **Checking Satisfiability of First-Order Formulas by Incremental Translation to SAT.**  
Barrett, Clark, W., Dill, David, L., Stump, A.  
edited by Brinksma, E., Larsen, K. G.  
2002
- **Using formal specifications for functional validation of hardware designs** *IEEE Design & Test of Computers*  
Shimizu, K., Dill, David, L.  
2002; 4 (19): 96–106
- **Deriving a simulation input generator and a coverage metric from a formal specification** *39th Design Automation Conference*  
Shimizu, K., Dill, D. L.  
ASSOC COMPUTING MACHINERY.2002: 801–806
- **Deciding Presburger arithmetic by model checking and comparisons with other methods** *4th International Conference on Formal Methods in Computer-Aided Design (FMCAD 2002)*

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- Ganesh, V., Berezin, S., Dill, D. L.  
SPRINGER-VERLAG BERLIN.2002: 171–186
- **Parallelizing the Mur phi verifier** *9th International Conference on Computer-Aided Verification (CAV 97)*  
Stern, U., Dill, D. L.  
SPRINGER.2001: 117–29
  - **A simple method for extracting models from protocol code** *28th Annual International Symposium on Computer Architecture*  
Lie, D., Chou, A., Engler, D., Dill, D. L.  
IEEE COMPUTER SOC.2001: 192–203
  - **A decision procedure for an extensional theory of arrays** *16th Annual IEEE Symposium on Logic in Computer Science*  
Stump, A., Barrett, C. W., Dill, D. L., LEVITT, J.  
IEEE COMPUTER SOC.2001: 29–37
  - **Successive approximation of abstract transition relations** *16th Annual IEEE Symposium on Logic in Computer Science*  
Das, S., Dill, D. L.  
IEEE COMPUTER SOC.2001: 51–58
  - **Automatic checking of aggregation abstractions through state enumeration** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*  
Park, S., Das, S., Dill, D. L.  
2000; 19 (10): 1202-1210
  - **Monitor-based formal specification of PCI** *3rd International Conference on Formal Methods in Computer-Aided Design*  
Shimizu, K., Dill, D. L., Hu, A. J.  
SPRINGER-VERLAG BERLIN.2000: 335–353
  - **Reliable verification using symbolic simulation with scalar values** *37th Annual Design Automation Conference (DAC)*  
Wilson, C., Dill, D. L.  
ASSOC COMPUTING MACHINERY.2000: 124–129
  - **Counterexample-guided choice of projections in approximate symbolic model checking** *IEEE/ACM International Conference on Computer Aided Design (ICCAD-2000)*  
Govindaraju, S. G., Dill, D. L.  
IEEE.2000: 115–119
  - **Java model checking** *15th IEEE International Conference on Automated Software Engineering (ASE 2000)*  
Park, D. Y., Stern, U., Skakkebaek, J. U., Dill, D. L.  
IEEE COMPUTER SOC.2000: 253–256
  - **Symbolic simulation with approximate values** *3rd International Conference on Formal Methods in Computer-Aided Design*  
Wilson, C., Dill, D. L., Bryant, R. E.  
SPRINGER-VERLAG BERLIN.2000: 470–485
  - **A framework for cooperating decision procedures** *17th International Conference on Automated Deduction (CADE-17)*  
Barrett, C. W., Dill, D. L., Stump, A.  
SPRINGER-VERLAG BERLIN.2000: 79–98
  - **Timing analysis of asynchronous systems using time separation of events** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*  
Chakraborty, S. A., Yun, K. Y., Dill, D. L.  
1999; 18 (8): 1061-1076
  - **Verifying systems with replicated components in Mur phi** *FORMAL METHODS IN SYSTEM DESIGN*  
Ip, C. N., Dill, D. L.  
1999; 14 (3): 273-310
  - **Automatic synthesis of extended burst-mode circuits: Part I (specification and hazard-free implementations)** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*  
Yun, K. Y., Dill, D. L.



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- 1999; 18 (2): 101-117
- **An executable specification and verifier for relaxed memory order** *IEEE TRANSACTIONS ON COMPUTERS*  
Park, S. J., Dill, D. L.  
1999; 48 (2): 227-235
  - **Min-max timing analysis and an application to asynchronous circuits** *PROCEEDINGS OF THE IEEE*  
Chakraborty, S., Dill, D. L., Yun, K. Y.  
1999; 87 (2): 332-346
  - **Automatic synthesis of extended burst-mode circuits: Part II (automatic synthesis)** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*  
Yun, K. Y., Dill, D. L.  
1999; 18 (2): 118-132
  - **Timing analysis of asynchronous systems using time separation of events.** *IEEE Transactions on Computer-Aided Design*  
Chakraborty, S., Yun, Kenneth, Y., Dill, David, L.  
1999; 8 (18): 1061-1076
  - **Experience with predicate abstraction.**  
Das, S., Dill, David, L., Park, S.  
1999
  - **Automatic synthesis of extended burst-mode circuits: Part I (specification and hazard-free implementations).** *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*  
Yun, Kenneth, Y., Dill, David, L.  
1999; 2 (18): 101-117
  - **Improved approximate reachability using auxiliary state variables.**  
Govindaraju, Shankar, G., Dill, David, L., Bergmann, Jules, P.  
1999
  - **Automatic synthesis of extended burst-mode circuits: Part II (specification and hazard-free implementations).** *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*  
Yun, Kenneth, Y., Dill, David, L.  
1999; 2 (18): 118-132
  - **An executable specification, analyzer and verifier for RMO (relaxed memory order).** *IEEE Transactions on Computers*  
Park, S., Dill, David, L.  
1999; 2 (48): 227-335
  - **Verifying systems with replicated components in Mur#.** *Formal Methods in System Design*  
Ip, C., Norris., Dill, David, L.  
1999; 3 (14): 41-75
  - **BDD-based synthesis of extended burst-mode controllers** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*  
Yun, K. Y., Lin, B., Dill, D. L., Devadas, S.  
1998; 17 (9): 782-792
  - **Verification of cache coherence protocols by aggregation of distributed transactions** *8th Annual ACM Symposium on Parallel Algorithms and Architectures*  
Park, S., Dill, D. L.  
SPRINGER.1998: 355-76
  - **Using magnetic disk instead of main memory in the Mur phi verifier** *10th International Conference on Computer-Aided Verification (CAV 98)*  
Stern, U., Dill, D. L.  
SPRINGER-VERLAG BERLIN.1998: 172-183
  - **Reducing manual abstraction in formal verification of out-of-order execution.**  
Jones, Robert, B., Skakkebak, Jens, U., Dill, David, L.  
edited by Gopalakrishnan, G., Windley, P.

1998

- **Verification of cache coherence protocols by aggregation of distributed transactions.** *Theory of Computing Systems*  
Park, S., Dill, David, L.  
1998; 4 (31): 355–376
- **Bdd-based synthesis of extended burst-mode controllers.** *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*  
Yun, Kenneth, Y., Lin, B., Dill, David, L., Devadas, S.  
1998; 9 (17): 782–792
- **Formally verifying data and control with weak reachability invariants.**  
Su, Jeffrey, X., Dill, David, L., Skakkebaek, Jens, U.  
edited by Gopalakrishnan, G., Windley, P.  
1998
- **Checking properties of safety critical specifications using efficient decision procedures.**  
Park, David, Y.W., Skakkebaek, Jens, U., Heimdahl, Mats, P.E., Czerny, Barbara, J., Dill, David, L.  
1998
- **A decision procedure for bit-vector arithmetic** *35th Design Automation Conference*  
Barrett, C. W., Dill, D. L., LEVITT, J. R.  
ASSOC COMPUTING MACHINERY.1998: 522–527
- **Verification by approximate forward and backward reachability** *IEEE/ACM International Conference on Computer-Aided Design*  
Govindaraju, S. G., Dill, D. L.  
ASSOC COMPUTING MACHINERY.1998: 366–370
- **Static analysis to identify invariants in RSML specifications** *5th International Symposium on Formal Techniques in Real-Time and Fault-Tolerant Systems (FTRTFT 98)*  
Park, D. Y., Skakkebaek, J. U., Dill, D. L.  
SPRINGER-VERLAG BERLIN.1998: 133–142
- **Format verification of out-of-order execution using incremental flushing** *10th International Conference on Computer-Aided Verification (CAV 98)*  
Skakkebaek, J. U., Jones, R. B., Dill, D. L.  
SPRINGER-VERLAG BERLIN.1998: 98–109
- **Practical timing analysis of asynchronous circuits using time separation of events** *IEEE Custom Integrated Circuits Conference*  
Chakraborty, S., Yun, K. Y., Dill, D. L.  
IEEE.1998: 455–458
- **Approximate reachability with BDDs using overlapping projections** *35th Design Automation Conference*  
Govindaraju, S. G., Dill, D. L., Hu, A. J., Horowitz, M. A.  
ASSOC COMPUTING MACHINERY.1998: 451–456
- **What's between simulation and formal verification? (Extended abstract)** *35th Design Automation Conference*  
Dill, D. L.  
ASSOC COMPUTING MACHINERY.1998: 328–329
- **Validation with guided search of the state space** *35th Design Automation Conference*  
Yang, C. H., Dill, D. L.  
ASSOC COMPUTING MACHINERY.1998: 599–604
- **Timing analysis for extended burst-mode circuits** *3rd International Symposium on Advanced Research in Asynchronous Circuits and Systems*  
Chakraborty, S., Dill, D. L., Yun, K. Y., Chang, K. Y.  
IEEE, COMPUTER SOC PRESS.1997: 101–111
- **Approximate algorithms for time separation of events** *1997 IEEE/ACM International Conference on Computer-Aided Design (ICCAD 97)*  
Chakraborty, S., Dill, D. L.  
IEEE, COMPUTER SOC PRESS.1997: 190–194

- **More accurate polynomial-time min-max timing simulation** *3rd International Symposium on Advanced Research in Asynchronous Circuits and Systems*  
Chakraborty, S., Dill, D. L.  
IEEE, COMPUTER SOC PRESS.1997: 112–123
- **Parallelizing the Mur phi verifier** *9th International Conference on Computer-Aided Verification (CAV 97)*  
Stern, U., Dill, D. L.  
SPRINGER-VERLAG BERLIN.1997: 256–267
- **Better verification through symmetry** *FORMAL METHODS IN SYSTEM DESIGN*  
Ip, C. N., Dill, D. L.  
1996; 9 (1-2): 41-75
- **State reduction using reversible rules** *33rd Design Automation Conference*  
Ip, C. N., Dill, D. L.  
ASSOC COMPUTING MACHINERY.1996: 564–567
- **Verification of flash cache coherence protocol by aggregation of distributed actions.**  
Park, S., Dill, David, L.  
1996
- **Combining state space caching and hash compaction.** *In Methoden des Entwurfs und der Verifikation digitaler Systeme, 4. GI/ITG/GME Workshop*  
Stern, U., Dill, D., L.  
1996
- **Formal methods: state of the art and future directions.** *ACM Computing Surveys*  
Clarke, E., M., Wing, J., M., Alur, R., Cleaveland, R., Dill, D., Emerson, A.  
1996; 4 (28): 626–43
- **The mur# verification system.**  
Dill, David, L.  
1996
- **Protocol verification by aggregation of distributed transactions.**  
Park, S., Dill, David, L.  
1996
- **A new scheme for memory-efficient probabilistic verification.**  
Stern, U., Dill, David, L.  
1996
- **Automata-theoretic verification of real-time systems.** *Formal Methods for Real-time Computing, number 5 in Trends in Software*  
Alur, R., Dill, David, L.  
edited by Heitmeyer, C., Mandrioli, D.  
1996: 55–81
- **Protocol verification by aggregation of distributed actions.**  
Park, S., Dill, David, L.  
1996
- **Combining state space caching and hash compaction.**  
Stern, U., Dill, David, L.  
1996
- **Better verification through symmetry.** *Formal Methods in System Design*  
Ip, C., Norris., Dill, David, L.  
1996; 1–2 (9): 41–75
- **Validity checking for combinations of theories with equality** *1st International Conference on Formal Methods in Computer-Aided Design (FMCAD 96)*  
Barrett, C., Dill, D., LEVITT, J.  
SPRINGER-VERLAG BERLIN.1996: 187–201

- **Self-consistency checking** *1st International Conference on Formal Methods in Computer-Aided Design (FMCAD 96)*  
Jones, R. B., Seger, C. J., Dill, D. L.  
SPRINGER-VERLAG BERLIN.1996: 159–171
- **Automatic generation of invariants in processor verification** *1st International Conference on Formal Methods in Computer-Aided Design (FMCAD 96)*  
Su, J. X., Dill, D. L., Barrett, C. W.  
SPRINGER-VERLAG BERLIN.1996: 377–388
- **EXACT 2-LEVEL MINIMIZATION OF HAZARD-FREE LOGIC WITH MULTIPLE-INPUT CHANGES** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*  
Nowick, S. M., Dill, D. L.  
1995; 14 (8): 986-997
- **Architecture validation for processors** *22nd Annual International Symposium on Computer Architecture*  
Ho, R. C., Yang, C. H., Horowitz, M. A., Dill, D. L.  
ASSOC COMPUTING MACHINERY.1995: 404–413
- **A high-performance asynchronous SCSI controller** *International Conference on Computer Design - VLSI in Computers and Processors (ICCD 95)*  
Yun, K. Y., Dill, D. L.  
IEEE COMPUTER SOC.1995: 44–49
- **Exact two-level minimization of hazard-free logic with multiple-input changes.** *IEEE Transactions on Computer-Aided Design of Integrated Circuits*  
Nowick, S., M., Dill, D., L.  
1995; 8 (14): 986–997
- **A high-performance asynchronous SCSI controller.**  
Yun, Kenneth, Y., Dill, David, L.  
1995
- **A theory of timed automata.** *Theoretical Computer Science*  
Alur, R., Dill, D., L.  
1995; 126: 183–235
- **Efficient validity checking for processor verification** *1995 IEEE/ACM International Conference on Computer-Aided Design*  
Jones, R. B., Dill, D. L., Burch, J. R.  
IEEE, COMPUTER SOC PRESS.1995: 2–6
- **Verification of real-time systems by successive over and under approximation** *7th Conference on Computer Aided Verification (CAV 95)*  
Dill, D. L., WONGTOI, H.  
SPRINGER-VERLAG BERLIN.1995: 409–422
- **Improved probabilistic verification by hash compaction** *IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods (CHARME 95)*  
Stern, U., Dill, D. L.  
SPRINGER-VERLAG BERLIN.1995: 206–224
- **Automatic verification of the SCI cache coherence protocol** *IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods (CHARME 95)*  
Stern, U., Dill, D. L.  
SPRINGER-VERLAG BERLIN.1995: 21–34
- **A THEORY OF TIMED AUTOMATA** *THEORETICAL COMPUTER SCIENCE*  
Alur, R., Dill, D. L.  
1994; 126 (2): 183-235
- **SYMBOLIC MODEL CHECKING FOR SEQUENTIAL-CIRCUIT VERIFICATION** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*  
Burch, J. R., Clarke, E. M., Long, D. E., McMillan, K. L., Dill, D. L.  
1994; 13 (4): 401-424

- **SELF-TIMED LOGIC USING CURRENT-SENSING COMPLETION DETECTION (CSCD)** *JOURNAL OF VLSI SIGNAL PROCESSING*  
Dean, M. E., Dill, D. L., Horowitz, M.  
1994; 7 (1-2): 7-16
- **NEW TECHNIQUES FOR EFFICIENT VERIFICATION WITH IMPLICITLY CONJOINED BDDS** *31st Design Automation Conference*  
Hu, A. J., York, G., Dill, D. L.  
ASSOC COMPUTING MACHINERY.1994: 276-282
- **PERFORMANCE-DRIVEN SYNTHESIS OF ASYNCHRONOUS CONTROLLERS** *1994 IEEE/ACM International Conference on Computer-Aided Design*  
Yun, K. Y., Lin, B., Dill, D. L., Devadas, S.  
IEEE COMPUTER SOC.1994: 550-557
- **Conference on Computer-Aided Verification, of Lecture Notes in Computer Science**  
edited by Dill, D. L.  
1994
- **Performance-driven synthesis of asynchronous controllers.**  
Yun, K., Y., Lin, B., Dill, D. L., Devadas, S.  
1994
- **Symbolic model checking for sequential circuit verification.** *IEEE Transactions on Computer-Aided Design of Integrated Circuits*  
Burch, Jerry, R., Clarke, Edmund, M., Long, David, E., McMillan, Kenneth, L., Dill, David, L.  
1994; 4 (13): 401-424
- **Automatic verification of pipelined microprocessor control.**  
Burch, Jerry, R., Dill, David, L.  
edited by Dill, D. L.  
1994
- **Self-timed logic using current sensing completion detection (CSCD).** *Journal of VLSI Signal Processing*  
Dean, M., Dill, David, L., Horowitz, M.  
1994; 1-2 (7): 7-16
- **THE DESIGN OF A HIGH-PERFORMANCE CACHE CONTROLLER - A CASE-STUDY IN ASYNCHRONOUS SYNTHESIS** *INTEGRATION-THE VLSI JOURNAL*  
Nowick, S. M., Dean, M. E., Dill, D. L., Horowitz, M.  
1993; 15 (3): 241-262
- **MODEL-CHECKING IN DENSE REAL-TIME INFORMATION AND COMPUTATION**  
Alur, R., Courcoubetis, C., Dill, D.  
1993; 104 (1): 2-34
- **UNIFYING SYNCHRONOUS ASYNCHRONOUS STATE MACHINE SYNTHESIS** *1993 IEEE/ACM International Conference on Computer-Aided Design*  
Yun, K. Y., Dill, D. L.  
IEEE, COMPUTER SOC PRESS.1993: 255-260
- **EFFICIENT VERIFICATION OF SYMMETRICAL CONCURRENT SYSTEMS** *1993 IEEE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN : VLSI IN COMPUTERS AND PROCESSES*  
Ip, C. N., Dill, D. L.  
IEEE, COMPUTER SOC PRESS.1993: 230-234
- **AUTOMATIC TECHNOLOGY MAPPING FOR GENERALIZED FUNDAMENTAL-MODE ASYNCHRONOUS DESIGNS** *30TH DESIGN AUTOMATION CONF*  
Siegel, P., Demicheli, G., Dill, D.  
ASSOC COMPUTING MACHINERY.1993: 61-67
- **Efficient verification of bdds using implicitly conjoined invariants.**  
Hu, Alan, J., Dill, David, L.  
1993

- **Higher-level specification and verification with BDDs.**  
Hu, Alan, J., Dill, David, L., Drexler, Andreas, J., Yang, C., Han  
1993
- **Automatic technology mapping for generalized fundamental-mode asynchronous designs**  
Siegel, P., Micheli, G. D., Dill, D.  
1993
- **Automatic technology mapping for generalized fundamental-mode asynchronous designs.** *Technical Report CSL-TR-93-580, Stanford University Computer Systems Laboratory*  
Siegel, P., Micheli, G. D., Dill, D.  
1993
- **Model-Checking for Real-Time Systems.** *Information and Computation*  
Alur, R., Courcoubetis, C., Dill, D.  
1993; 1 (104): 2–34
- **Practical generalizations of asynchronous state machines.**  
Yun, Kenneth, Y., Dill, David, L., Nowick, Steven, M.  
1993
- **The design of a high-performance cache controller: a case study in asynchronous synthesis.** *Integration: the VLSI Journal*  
Nowick, S., M., Dean, M., E., Dill, D., L., Horowitz, M.  
1993; 3 (15): 241–262
- **Reducing BDD size by exploiting functional dependencies.**  
Hu, Alan, J., Dill, David, L.  
1993
- **Efficient verification of symmetric concurrent systems.**  
Ip, C. N., Dill, David, L.  
1993
- **BETTER VERIFICATION THROUGH SYMMETRY** *IFIP WG10.2 International Conference on Computer Hardware Description Languages and their Applications (CHDL 93)*  
Ip, C. N., Dill, D. L.  
ELSEVIER SCIENCE BV.1993: 97–111
- **MODELING HIERARCHICAL COMBINATIONAL-CIRCUITS** *1993 IEEE/ACM International Conference on Computer-Aided Design*  
Burch, J. R., Dill, D., Wolf, E., Demicheli, G.  
I E E E, COMPUTER SOC PRESS.1993: 612–617
- **FORMAL SPECIFICATION OF ABSTRACT MEMORY MODELS** *Symposium on Research on Integrated Systems*  
Dill, D. L., Park, S., Nowatzky, A. G.  
M I T PRESS.1993: 38–52
- **SYMBOLIC MODEL CHECKING - 1020 STATES AND BEYOND** *5TH SYMP ON LOGIC IN COMPUTER SCIENCE*  
Burch, J. R., Clarke, E. M., McMillan, K. L., Dill, D. L., Hwang, L. J.  
ACADEMIC PRESS INC JNL-COMP SUBSCRIPTIONS.1992: 142–70
- **CHECKING FOR LANGUAGE INCLUSION USING SIMULATION PREORDERS** *LECTURE NOTES IN COMPUTER SCIENCE*  
Dill, D. L., Hu, A. J., WONGTOI, H.  
1992; 575: 255-265
- **ALGORITHMS FOR INTERFACE TIMING VERIFICATION** *1992 IEEE INTERNATIONAL CONF ON COMPUTER DESIGN : VLSI IN COMPUTERS & PROCESSORS ( ICCD 92 )*  
McMillan, K. L., Dill, D. L.  
I E E E, COMPUTER SOC PRESS.1992: 48–51
- **MINIMIZATION OF TIMED TRANSITION-SYSTEMS** *3RD INTERNATIONAL CONF ON CONCURRENCY THEORY*

- 
- Alur, R., Courcoubetis, C., Halbwachs, N., Dill, D., WONGTOI, H.  
SPRINGER-VERLAG BERLIN.1992: 340–354
- **CHECKING FOR LANGUAGE INCLUSION USING SIMULATION PREORDERS** *3RD INTERNATIONAL WORKSHOP ON COMPUTER AIDED VERIFICATION ( CAV 91 )*  
Dill, D. L., Hu, A. J., WONGTOI, H.  
SPRINGER-VERLAG BERLIN.1992: 255–265
  - **PRACTICAL ASYNCHRONOUS CONTROLLER-DESIGN** *1992 IEEE INTERNATIONAL CONF ON COMPUTER DESIGN : VLSI IN COMPUTERS & PROCESSORS ( ICCD 92 )*  
Nowick, S. M., Yun, K. Y., Dill, D. L.  
I E E E, COMPUTER SOC PRESS.1992: 341–345
  - **SYNTHESIS OF 3D ASYNCHRONOUS STATE MACHINES** *1992 IEEE INTERNATIONAL CONF ON COMPUTER DESIGN : VLSI IN COMPUTERS & PROCESSORS ( ICCD 92 )*  
Yun, K. Y., Dill, D. L., Nowick, S. M.  
I E E E, COMPUTER SOC PRESS.1992: 346–350
  - **AN IMPLEMENTATION OF 3 ALGORITHMS FOR TIMING VERIFICATION BASED ON AUTOMATA EMPTINESS** *CONF ON REAL-TIME SYSTEMS SYMP*  
Alur, R., Courcoubetis, C., Dill, D., Halbwachs, N., WONGTOI, H.  
I E E E, COMPUTER SOC PRESS.1992: 157–166
  - **Synthesis of 3D asynchronous state machines.**  
Yun, Kenneth, Y., Dill, David, L.  
1992
  - **Protocol verification as a hardware design aid.**  
Dill, David, L., Drexler, Andreas, J., Hu, Alan, J., Yang, C., Han  
1992
  - **Practical asynchronous controller design.**  
Nowick, Steven, M., Yun, K., Dill, David, L.  
1992
  - **Algorithms for interface timing verification.**  
McMillan, K., Dill, David, L.  
1992
  - **Specification and automatic verification of self-timed queues** *Formal Methods in Systems Design*  
Dill, David, L., Nowick, Steven, M., Sproull, Robert, F.  
1992; 1 (1): 29–62
  - **Automatic synthesis of 3D asynchronous state machines.**  
Yun, Kenneth, Y., Dill, David, L.  
1992
  - **The theory of timed automata.** *In Real-Time: Theory in Practice, volume 600 of Lecture Notes in Computer Science*  
Alur, R., Dill, David, L.  
REX Workshop, Mook, The Netherlands.1992: 45–73
  - **Practical generalizations of asynchronous state machines.** *Technical Report CSL-TR-92-544, Computer Systems Laboratory, Stanford University*  
Yun, Kenneth, Y., Dill, David, L., Nowick, Steven, M.  
1992
  - **Formal Verification of Cache Systems using Refinement Relations.** *Formal Methods in Systems Design*  
Loewenstein, P., Dill, D.  
1992; 4 (1): 355–383
  - **Verification with real-time COSPAN.**  
Courcoubetis, C., Dill, D., Chatzaki, M., Tzounakis, P.

1992

- **An Implementation of Three Algorithms for Timing Verification Based on Automata Emptiness.**  
Alur, R., Courcoubetis, C., Dill, D., Halbwachs, N., Wong-Toi, H.  
1992
- **Verifying automata specifications of probabilistic real-time systems.** *In Real-Time: Theory in Practice, volume 600 of Lecture Notes in Computer Science*  
Alur, R., Courcoubetis, C., Dill, David, L.  
REX Workshop, Mook, The Netherlands.1992: 28–44
- **Symbolic model checking: 1020 states and beyond.** *Information and Computation*  
Burch, J., R., Clarke, E., M., McMillan, K., L., Dill, D., L., Hwang, L., J.  
1992; 2 (98): 142–170
- **THE THEORY OF TIMED AUTOMATA** *REX WORKSHOP ON REAL-TIME : THEORY IN PRACTICE*  
Alur, R., Dill, D.  
SPRINGER VERLAG.1992: 45–73
- **VERIFYING AUTOMATA SPECIFICATIONS OF PROBABILISTIC REAL-TIME SYSTEMS** *REX WORKSHOP ON REAL-TIME : THEORY IN PRACTICE*  
Alur, R., Courcoubetis, C., Dill, D.  
SPRINGER VERLAG.1992: 28–44
- **MINIMIZATION OF TIMED TRANSITION-SYSTEMS** *LECTURE NOTES IN COMPUTER SCIENCE*  
Alur, R., Courcoubetis, C., Halbwachs, N., Dill, D., WONGTOI, H.  
1992; 630: 340-354
- **MODEL-CHECKING FOR PROBABILISTIC REAL-TIME SYSTEMS** *LECTURE NOTES IN COMPUTER SCIENCE*  
Alur, R., Courcoubetis, C., Dill, D.  
1991; 510: 115-126
- **MODEL-CHECKING FOR PROBABILISTIC REAL-TIME SYSTEMS** *18TH INTERNATIONAL COLLOQUIUM ON AUTOMATA, LANGUAGES AND PROGRAMMING (ICALP 91)*  
Alur, R., Courcoubetis, C., Dill, D.  
SPRINGER-VERLAG BERLIN.1991: 115–126
- **SYNTHESIS OF ASYNCHRONOUS STATE MACHINES USING A LOCAL CLOCK** *INTERNATIONAL CONF ON COMPUTER DESIGN : VLSI IN COMPUTERS AND PROCESSORS*  
Nowick, S. M., Dill, D. L.  
I E E E, COMPUTER SOC PRESS.1991: 192–197
- **Synthesis of asynchronous state machines using a local clock.**  
Nowick, Steven, M., Dill, David, L.  
1991
- **Efficient self-timing with level-encoded two-phase dual rail (LEDR).**  
Dean, Mark, E., Williams, Ted, E., Dill, David, L.  
1991
- **Automatic synthesis of locally-clocked asynchronous state machines.**  
Nowick, Steven, M., Dill, David, L.  
1991
- **SELF-TIMED LOGIC USING CURRENT-SENSING COMPLETION DETECTION (CSCD)** *INTERNATIONAL CONF ON COMPUTER DESIGN : VLSI IN COMPUTERS AND PROCESSORS*  
Dean, M. E., Dill, D. L., Horowitz, M.  
I E E E, COMPUTER SOC PRESS.1991: 187–191
- **SYNTHESIZING PROCESSES AND SCHEDULERS FROM TEMPORAL SPECIFICATIONS** *2ND INTERNATIONAL CONF ON COMPUTER-AIDED VERIFICATION (CAV 90)*  
WONGTOI, H., Dill, D. L.



---

SPRINGER.1991: 272–281

- **COMPLETE TRACE STRUCTURES** *WORKSHOP ON HARDWARE SPECIFICATION, VERIFICATION AND SYNTHESIS : MATHEMATICAL ASPECTS*  
Dill, D. L.  
SPRINGER-VERLAG BERLIN.1990: 224–243
- **TIMING ASSUMPTIONS AND VERIFICATION OF FINITE-STATE CONCURRENT SYSTEMS** *LECTURE NOTES IN COMPUTER SCIENCE*  
Dill, D. L.  
1990; 407: 197-212
- **COMPLETE TRACE STRUCTURES** *LECTURE NOTES IN COMPUTER SCIENCE*  
Dill, D. L.  
1990; 408: 224-243
- **AUTOMATA FOR MODELING REAL-TIME SYSTEMS** *17TH INTERNATIONAL COLLOQUIUM ON AUTOMATA, LANGUAGES AND PROGRAMMING (ICALP 90)*  
Alur, R., Dill, D.  
SPRINGER-VERLAG.1990: 322–335
- **Symbolic model checking: 10 states and beyond.**  
Burch, J., R., Clarke, E., M., McMillan, K., L., Dill, D., L., Hwang, J.  
1990
- **Sequential circuit verification using symbolic model-checking.**  
Burch, J., R., Clarke, E., M., Dill, D., L., McMillan, K., L.  
1990
- **Specification and automatic verification of self-timed queues** *Formal Verification of Hardware Design*  
Dill, D. L., Nowick, S. M., Sproull, R. F.  
edited by Yoeli, M.  
IEEE Computer Society Press.1990: 225–248
- **Model-checking for real-time systems.**  
Alur, R., Courcoubetis, C., Dill, D.  
1990
- **Automatic verification of sequential circuits using temporal logic** *Formal Verification of Hardware Design.*  
Browne, M. C., Clarke, E. M., Dill, D. L., Mishra, B.  
edited by Yoeli, M.  
IEEE Computer Society Press.1990: 166–175
- **Automatic verification** *Synchronization Design for Digital Systems*  
Nowick, S. M., Dill, D. L.  
edited by Meng, T. H.  
Kluwer Academic Publishers.1990: 147–172
- **Automatic verification of asynchronous circuits using temporal logic.** *Formal Verification of Hardware Design, Reprint of a paper in IEE proceedings, Pt. E.*  
Dill, David, L., Clarke, Edmund, M.  
edited by Yoeli, M.  
IEEE Computer Society Press.1990: 176–183
- **AUTOMATA FOR MODELING REAL-TIME SYSTEMS** *LECTURE NOTES IN COMPUTER SCIENCE*  
Alur, R., Dill, D.  
1990; 443: 322-335
- **TIMING ASSUMPTIONS AND VERIFICATION OF FINITE-STATE CONCURRENT SYSTEMS** *INTERNATIONAL WORKSHOP ON AUTOMATIC VERIFICATION METHODS FOR FINITE STATE SYSTEMS*  
Dill, D. L.  
SPRINGER-VERLAG BERLIN.1990: 197–212

- **Complete trace structures** *In Hardware Specification, Verification and Synthesis: Mathematical Aspects, volume 408 of Lecture Notes in Computer Science*  
Dill, D. L.  
1989: 224–243
- **PRACTICALITY OF STATE-MACHINE VERIFICATION OF SPEED-INDEPENDENT CIRCUITS** *1989 IEEE INTERNATIONAL CONF ON COMPUTER-AIDED DESIGN : A CONF FOR THE EE CAD PROFESSIONAL ( ICCAD-89 )*  
Nowick, S. M., Dill, D. L.  
IEEE, COMPUTER SOC PRESS.1989: 266–269
- **AUTOMATIC VERIFICATION OF SPEED-INDEPENDENT CIRCUITS WITH PETRI NET SPECIFICATIONS** *1989 IEEE INTERNATIONAL CONF ON COMPUTER DESIGN : VLSI IN COMPUTERS AND PROCESSORS*  
Dill, D. L., Nowick, S. M., SPROULL, R. F.  
IEEE.1989: 212–216
- **Practicality of state-machine verification of speed-independent circuits.**  
Nowick, Steven, M., Dill, David, L.  
1989
- **Automatic verification of speed-independent circuits with Petri net specifications.**  
Dill, David, L., Nowick, Steven, M., Sproull, Robert, F.  
1989
- **Trace Theory for Automatic Hierarchical Verification of Speed-independent Circuits**  
edited by Dill, D. L.  
MIT Press.1989
- **Specification and automatic verification of self-timed queues.** *Technical Report CSL-TR-89-387, Computer Systems Laboratory, Stanford University, This was reprinted in the IEEE tutorial: Formal Verification of Hardware Design, by Michael Yoeli*  
Dill, David, L., Nowick, Steven, M., Sproull, Robert, F.  
1989
- **Trace theory for automatic hierarchical verification of speed-independent circuits.**  
Dill, David, L.  
1988
- **AUTOMATIC VERIFICATION OF SEQUENTIAL-CIRCUITS USING TEMPORAL LOGIC** *IEEE TRANSACTIONS ON COMPUTERS*  
Browne, M. C., Clarke, E. M., Dill, D. L., Mishra, B.  
1986; 35 (12): 1035-1044
- **AUTOMATIC VERIFICATION OF ASYNCHRONOUS CIRCUITS USING TEMPORAL LOGIC** *IEE PROCEEDINGS-E COMPUTERS AND DIGITAL TECHNIQUES*  
Dill, D. L., Clarke, E. M.  
1986; 133 (5): 276-282
- **Automatic verification of sequential circuits using temporal logic.** *IEEE Transactions on Computers, This was reprinted in the IEEE tutorial: Formal Verification of Hardware Design, by Michael Yoeli*  
Browne, Michael, C., Clarke, Edmund, M., Dill, David, L., Mishra, B.  
1986; 12 (C-35): 1035–1044
- **Automatic circuit verification using temporal logic: Two new examples.**  
Browne, Michael, C., Clarke, Edmund, M., Dill, David, L.  
1986
- **Automatic verification of asynchronous circuits using temporal logic**  
Dill, David, L., Clark, Edmund, M.  
1986
- **Automatic verification of asynchronous circuits using temporal logic.** *Technical Report CMU-CS-85-125, Department of Computer Science, Carnegie-Mellon University*  
Dill, David, L., Clarke, Edmund, M.

1985

- **Automatic verification of sequential circuits using temporal logic.**

Browne, Michael, C., Clarke, Edmund, M., Dill, David, L., Mishra, B.

1985

- **Checking the correctness of sequential circuits.**

Browne, Michael, C., Clarke, Edmund, M., Dill, David, L.

1985

- **Automatic verification of asynchronous circuits using temporal logic.**

Dill, David, L., Clarke, Edmund, M.

1985

- **Automatic verification of sequential circuits using temporal logic.** *Technical Report CMU-CS-85-100, Department of Computer Science, Carnegie-Mellon University*

Browne, Michael, C., Clarke, Edmund, M., Dill, David, L., Mishra, B.

1984