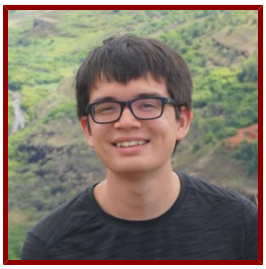
Stanford



Jeff Setter

Ph.D. Student in Electrical Engineering, admitted Autumn 2015

Bio

BIO

Jeff is a Ph.D. candidate at Stanford University in Electrical Engineering advised by Mark Horowitz. His research interests are in building hardware accelerators from software languages. Halide to Hardware is a project to use a data-parallel functional program formerly developed for CPU programs to produce hardware. Through the AHA hardware toolflow, these image processing and deep learning algorithms are mapped to a CGRA. Previously, Jeff received a B.S. in Electrical and Computer Engineering from Cornell University in 2015.

Publications

PUBLICATIONS

- **Interstellar: Using Halide's Scheduling Language to Analyze DNN Accelerators**
  Yang, X., Gao, M., Liu, Q., Setter, J., Pu, J., Nayak, A., Bell, S., Cao, K., Ha, H., Raina, P., Kozyrakis, C., Horowitz, M., ACM
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- **Creating an Agile Hardware Design Flow**
  Bahr, R., Barrett, C., Bhagdikar, N., Carsello, A., Daly, R., Donovick, C., Durst, D., Fatahalian, K., Feng, K., Hanrahan, P., Hofstee, T., Horowitz, M., Huff, et al
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- **Programming Heterogeneous Systems from an Image Processing DSL** *ACM TRANSACTIONS ON ARCHITECTURE AND CODE OPTIMIZATION*
  Pu, J., Bell, S., Yang, X., Setter, J., Richardson, S., Ragan-Kelley, J., Horowitz, M.
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