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Bio

BIO

I'm an EE PhD candidate at Stanford University supervised by Prof. H.-S. Philip Wong. My current research interests focus on in-memory computing enabled by emerging memory technologies (e.g., 3D vertical RRAM), with technical efforts spanning from device characterization and cross-stack modeling, to efficient architectures and their hardware realizations.

Published more than 30 papers appearing in top conferences (IEDM, ISSCC, VLSI, DAC) and journals (JSSC, Nature Electronics), including several invited papers. Our research has been featured on EE Times, Forbes, Storage Newsletter, Stanford News, ScienceNet, and PKU News. Meanwhile, I serve as an active reviewer for JSSC, Scientific Reports, EDL, T-ED, Applied Physics Letters, T-CAD, T-VLSI, and several IEEE conferences.

I'm a recipient of 2016 IEEE EDS Masters Student Fellowship, Best Paper Award at 2016 SRC TECHCON, 'Golden List of Reviewers' by IEEE EDL and T-ED, and nomination for Best Student Paper Award at 2016 Symposium of VLSI Technology.

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- Homepage: https://www.haitongli.me/
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Publications

PUBLICATIONS

- **Next-Generation Ultrahigh-Density 3-D Vertical Resistive Switching Memory (VRSM)-Part I: Accurate and Computationally Efficient Modeling** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Qin, S., Jiang, Z., Li, H., Fujii, S., Lee, D., Wong, S., Wong, H.
  2019; 66 (12): 5139–46
- **Next-Generation Ultrahigh-Density 3-D Vertical Resistive Switching Memory (VRSM)-Part II: Design Guidelines for Device, Array, and Architecture** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Jiang, Z., Qin, S., Li, H., Fujii, S., Lee, D., Wong, S., Wong, H.
  2019; 66 (12): 5147–54
- **Device and materials requirements for neuromorphic computing** *JOURNAL OF PHYSICS D-APPLIED PHYSICS*
  Islam, R., Li, H., Chen, P., Wan, W., Chen, H., Gao, B., Wu, H., Yu, S., Saraswat, K., Wong, H.
  2019; 52 (11)

- **Ternary content-addressable memory with MoS2 transistors for massively parallel data search** *NATURE ELECTRONICS*
  Yang, R., Li, H., Smithe, K. H., Kim, T. R., Okabe, K., Pop, E., Fan, J. A., Wong, H.
  2019; 2 (3): 108–14
- **A 43pJ/Cycle Non-Volatile Microcontroller with 4.7 mu s Shutdown/Wake-up Integrating 2.3-bit/Cell Resistive RAM and Resilience Techniques**
  Wu, T. F., Le, B. Q., Radway, R., Bartolo, A., Hwang, W., Jeong, S., Li, H., Tandon, P., Vianello, E., Vivet, P., Nowak, E., Wootters, M. K., Wong, et al
  IEEE.2019: 226-+
- **On-Chip Memory Technology Design Space Explorations for Mobile Deep Neural Network Accelerators**
  Li, H., Bhargava, M., Whatmough, P. N., Wong, H., ACM
  ASSOC COMPUTING MACHINERY.2019
- **Neuro-inspired computing with emerging memories: where device physics meets learning algorithms**
  Li, H., Raina, P., Wong, H., Drouhin, H. J., Wegrowe, J. E., Razeghi, M., Jaffres, H.
  SPIE-INT SOC OPTICAL ENGINEERING.2019
- **Recommended Methods to Study Resistive Switching Devices** *ADVANCED ELECTRONIC MATERIALS*
  Lanza, M., Wong, H., Pop, E., Ielmini, D., Strukov, D., Regan, B. C., Larcher, L., Villena, M. A., Yang, J., Goux, L., Belmonte, A., Yang, Y., Puglisi, et al
  2019; 5 (1)
- **Hyperdimensional Computing Exploiting Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D Integration** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Wu, T. F., Li, H., Huang, P., Rahimi, A., Hills, G., Hodson, B., Hwang, W., Rabaey, J. M., Wong, H., Shulaker, M. M., Mitra, S.
  2018; 53 (11): 3183–96
- **Electronic synapses made of layered two-dimensional materials** *NATURE ELECTRONICS*
  Shi, Y., Liang, X., Yuan, B., Chen, V., Li, H., Hui, F., Yu, Z., Yuan, F., Pop, E., Wong, H., Lanza, M.
  2018; 1 (8): 458–65
- **Brain-Inspired Computing Exploiting Carbon Nanotube FETs and Resistive RAM: Hyperdimensional Computing Case Study**
  Wu, T. F., Li, H., Huang, P., Rahimi, A., Rabaey, J. M., Wong, H., Shulaker, M. M., Mitra, S., IEEE
  IEEE.2018
- **Brain-Inspired Computing Exploiting Carbon Nanotube FETs and Resistive RAM: Hyperdimensional Computing Case Study**
  Wu, T. F., Li, H., Huang, P., Rahimi, A., Rabaey, J. M., Wong, H., Shulaker, M. M., Mitra, S., IEEE
  IEEE.2018: 492-+
- **First Principles Study of Memory Selectors using Heterojunctions of 2D Layered Materials**
  Li, L., Magyari-Kope, B., Wang, C., Deshmukh, S., Jiang, Z., Li, H., Yang, Y., Li, H., Tian, H., Pop, E., Ren, T., Wong, H., IEEE
  IEEE.2018
- **Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM**
  Jiang, Z., Qin, S., Li, H., Fujii, S., Lee, D., Wong, S., Wong, H., IEEE
  IEEE.2018: 107–8
- **Device and Circuit Interaction Analysis of Stochastic Behaviors in Cross-Point RRAM Arrays** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Li, H., Huang, P., Gao, B., Liu, X., Kang, J., Wong, H.
  2017; 64 (12): 4928–36
- **2D Molybdenum Disulfide (MoS2) Transistors Driving RRAMs with 1T1R Configuration**
  Yang, R., Li, H., Smithe, K. H., Kim, T. R., Okabe, K., Pop, E., Fan, J. A., Wong, H., IEEE
  IEEE.2017
- **Design and Application of Oxide-Based Resistive Switching Devices for Novel Computing Architectures** *IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY*
  Kang, J., Huang, P., Gao, B., Li, H., Chen, Z., Zhao, Y., Liu, C., Liu, L., Liu, X.
  2016; 4 (5): 307-313
- **Disturbance characteristics of half-selected cells in a cross-point resistive switching memory array** *NANOTECHNOLOGY*
  Chen, Z., Li, H., Chen, H., Chen, B., Liu, R., Huang, P., Zhang, F., Jiang, Z., Ye, H., Gao, B., Liu, L., Liu, X., Kang, et al

2016; 27 (21)

- **3-D Resistive Memory Arrays: From Intrinsic Switching Behaviors to Optimization Guidelines** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Li, H., Gao, B., Chen, H. (., Chen, Z., Huang, P., Liu, R., Zhao, L., Jiang, Z. (., Liu, L., Liu, X., Yu, S., Kang, J., Nishi, et al
  2015; 62 (10): 3160-3167

- **A learnable parallel processing architecture towards unity of memory and computing** *SCIENTIFIC REPORTS*
  Li, H., Gao, B., Chen, Z., Zhao, Y., Huang, P., Ye, H., Liu, L., Liu, X., Kang, J.
  2015; 5

- **Analysis of the Voltage-Time Dilemma of Metal Oxide-Based RRAM and Solution Exploration of High Speed and Low Voltage AC Switching** *IEEE TRANSACTIONS ON NANOTECHNOLOGY*
  Huang, P., Wang, Y., Li, H., Gao, B., Chen, B., Zhang, F., Zeng, L., Du, G., Kang, J., Liu, X.
  2014; 13 (6): 1127-1132

- **A SPICE Model of Resistive Random Access Memory for Large-Scale Memory Array Simulation** *IEEE ELECTRON DEVICE LETTERS*
  Li, H., Huang, P., Gao, B., Chen, B., Liu, X., Kang, J.
  2014; 35 (2): 211-213

- **Write Disturb Analyses on Half-Selected Cells of Cross-Point RRAM Arrays** *International Reliability Physics Symposium (IRPS)*
  Li, H., Chen, H., Chen, Z., Chen, B., Liu, R., Qiu, G., Huang, P., Zhang, F., Jiang, Z., Gao, B., Liu, L., Liu, X., Yu, et al
  IEEE.2014

- **Statistical Assessment Methodology for the Design and Optimization of Cross-Point RRAM Arrays** *IEEE 6th International Memory Workshop (IMW)*
  Li, H., Jiang, Z., Huang, P., Chen, H., Chen, B., Liu, R., Chen, Z., Zhang, F., Liu, L., Gao, B., Liu, X., Yu, S., Wong, et al
  IEEE.2014

- **Impact of Pulse Rise Time on Programming of Cross-Point RRAM Arrays** *PROCEEDINGS OF TECHNICAL PROGRAM - 2014 INTERNATIONAL SYMPOSIUM ON VLSI TECHNOLOGY, SYSTEMS AND APPLICATION (VLSI-TSA)*
  Liu, R., Chen, H., Li, H., Huang, P., Zhao, L., Chen, Z., Zhang, F., Chen, B., Liu, L., Liu, X., Gao, B., Yu, S., Nishi, et al
  2014

- **Parameters Extraction on HfOX based RRAM** *PROCEEDINGS OF THE 2014 44TH EUROPEAN SOLID-STATE DEVICE RESEARCH CONFERENCE (ESSDERC 2014)*
  Huang, P., Chen, B., Li, H., Chen, Z., Gao, B., Liu, X., Kang, J.
  2014: 250-253

- **A Physics-Based Compact Model of Metal-Oxide-Based RRAM DC and AC Operations** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Huang, P., Liu, X. Y., Chen, B., Li, H. T., Wang, Y. J., Deng, Y. X., Wei, K. L., Zeng, L., Gao, B., Du, G., Zhang, X., Kang, J. F.
  2013; 60 (12): 4090-4097