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Publications

PUBLICATIONS

- **Gap-free Processor Verification by S(2)QED and Property Generation**
  Devarajegowda, K., Fadiheh, M., Singh, E., Barrett, C., Mitra, S., Ecker, W., Stoffel, D., Kunz, W., DiNatale, G., Bolchini, C., Vatajelu, E. I.
  IEEE.2020: 526–31

- **Symbolic QED Pre-silicon Verification for Automotive Microcontroller Cores: Industrial Case Study**
  Singh, E., Devarajegowda, K., Simon, S., Schnieder, R., Ganesan, K., Fadiheh, M., Stoffel, D., Kunz, W., Barrett, C., Ecker, W., Mitra, S., IEEE
  IEEE.2019: 1000–1005

- **Unlocking the Power of Formal Hardware Verification with CoSA and Symbolic QED**
  Lonsing, F., Ganesan, K., Mann, M., Nuthakki, S., Singh, E., Srouji, M., Yang, Y., Mitra, S., Barrett, C., IEEE
  IEEE.2019

- **E-QED: Electrical Bug Localization During Post-silicon Validation Enabled by Quick Error Detection and Formal Methods**
  Singh, E., Barrett, C., Mitra, S., Majumdar, R., Kuncak
  SPRINGER INTERNATIONAL PUBLISHING AG.2017: 104–25

- **Symbolic Quick Error Detection for Pre-Silicon and Post-Silicon Validation: Frequently Asked Questions** *IEEE DESIGN & TEST*
  Singh, E., Lin, D., Barrett, C., Mitra, S.
  2016; 33 (6): 55-62

- **Exploiting Rotational Symmetries for Improved Stacked Yields in W2W 3D-SICs** *29th IEEE VLSI Test Symposium (VTS)/Workshop on Design for Reliability and Variability (DRV)*
  Singh, E.
  IEEE COMPUTER SOC.2011: 32–37