

Stanford



Robert Dutton

Robert and Barbara Kleist Professor in the School of Engineering
Electrical Engineering

Bio

BIO

Dutton's group develops and applies computer aids to process modeling and device analysis. His circuit design activities emphasize layout-related issues of parameter extraction and electrical behavior for devices that affect system performance. Activities include primarily silicon technology modeling both for digital and analog circuits, including OE/RF applications. New emerging area now includes bio-sensors and the development of computer-aided bio-sensor design.

ACADEMIC APPOINTMENTS

- Professor, Electrical Engineering

HONORS AND AWARDS

- J.J. Ebers Award, Institute of Electrical and Electronics Engineers (1987)
- Jack A. Morton Award, Institute of Electrical and Electronics Engineers (1996)
- SIA University Researcher Award, Semiconductor Industry Association (2000)
- Phil Kaufman Award, Electronic Design Automation Consortium (2006)

BOARDS, ADVISORY COMMITTEES, PROFESSIONAL ORGANIZATIONS

- member, National Academy of Engineering (1991 - present)
- Member, Semiconductor Industries Association (2005 - present)

PROFESSIONAL EDUCATION

- PhD, UC Berkeley (1970)

LINKS

- <http://www-tcad.stanford.edu/tcad/bios/dutton.html>: <http://www-tcad.stanford.edu/tcad/bios/dutton.html>

Teaching

COURSES

2019-20

- The Electrical Engineering Profession: EE 100 (Aut)

2018-19

- Analog Communications Design Laboratory: EE 133, EE 233 (Win)
- The Electrical Engineering Profession: EE 100 (Aut)

2017-18

- Analog Communications Design Laboratory: EE 133, EE 233 (Win)
- The Electrical Engineering Profession: EE 100 (Aut)

2016-17

- Analog Communications Design Laboratory: EE 133, EE 233 (Win)

STANFORD ADVISEES

Doctoral Dissertation Reader (AC)

Pin Pin Tea-makorn

Doctoral Dissertation Advisor (AC)

Tim Anderson

Publications

PUBLICATIONS

- **Proc. of the ICSSDP** *Simulation of Multilayer Structures for VLSI Using the SUPREM-III Process Simulation Program*
Hansen, S., E., Shott, J., D., Fahey, P., M., Plummer, J., D., Dutton, R., W., K.
edited by R.J., Board, D.
Pineridge Press.
- **Simulation of Integrated Circuits Design** *Process and Device Modeling for Integrated Circuit Design*
Antoniadis, D., A., Dutton, R., W.
- **New Challenges in Device Design for Integrated Electronic Systems**
Dutton, R., W., Yu, Z.
- **Analysis of Advanced Devices Using Industry-Networked Technology CAD (ALADDIN-CAD)** *Final Report, California Competitive Technology Program (CompTech Grant # C90-072).*
Dutton, R., W.
- **Workload Dependent NBTI and PBTI Analysis for a Sub-45nm Commercial Microprocessor** *IEEE IRPS, Anaheim, CA*
Mintarno, E., Chandra, V., Pietromonaco, D., Aitken, R., Dutton, R., W.
2013: 3A.1.1-3A.1.6
- **Applications of NanoNewton Dielectrophoretic Forces using Atomic Layer Deposited Oxides for Microfluidic Sample Preparation and Proteomics**
Emaminejad, S., Javanmard, M., Gupta, C., Dutton, R., W., Davis, R., W., Howe, R., T.
2013
- **Smart surfaces: Use of electrokinetics for selective modulation of biomolecular affinities**
Emaminejad, S., Javanmard, M., Dutton, R., W., Davis, R., W.
2012
- **Efficient Control of DNA Transport in Nanopore-based Nanofluidic Transistors**
Paik, K., H., Liu, Y., Tabard-Cossa, V., Huber, D., Provine, J., Howe, R., Dutton, R. W.
2011
- **An Electronic Microfluidic Switch using Dielectrophoresis for Control of Microparticles**
Javanmard, M., Emaminejad, S., Dutton, R., W., Davis, R.
2011
- **Smart Surfaces: Use of Electrokinetics for Selective Modulation of Biomolecular Affinities** *MRS Fall Meeting, Boston, MA*
Emaminejad, S., Javanmard, M., Dutton, R., W., Davis, R., W.
2011; 1414

- **Field Effect Resistor, a Single-Device-at-Pad Solution for ESD Protection in Deeply Scaled SOI Technology**
Cao, S., Salman, A., A., Chun, J., H., Beebe, S., G., Pelella, M., M., Dutton, R., W.
2010
- **Modeling and RF Analysis of Silicon Inter-band Tunnel Diode with THz Cut-off Frequency**
Kim, K., R., Kang, I., M., Dutton, R., W.
2010
- **Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering**
Cao, S., Chun, J., H., Choi, E., Beebe, S., Anderson, W., Dutton, R., W.
2010
- **Optimized Self-Tuning for Circuit Aging**
Mintarno, E., Skaf, J., Zheng, R., Velamala, J., Cao, Y., Boyd, S., Dutton, R. W.
2010
- **Electrical Modulation of Ion Concentration in Dual-Gated Nanochannels**
Liu, Y., Ran, Q., Dutton, R., W.
2010
- **ESD Design Challenges and Strategies in Deeply-Scaled Integrated Circuits**
Cao, S., Chen, T., W., Beebe, S., G., Dutton, R., W.
2009
- **Field Effect Diode for Effective CDM ESD Protection in 45nm SOI Technology**
Cao, S., Beebe, S., G., Salman, A., A., Pelella, M., M., Chun, J., H., Dutton, R., W.
2009
- **Numerical Flicker Noise Model for Dual Channel FETs**
Chen, C., Y., Liu, Y., Dutton, R., W., Sato-Iwanaga, J., Inoue, A., Sorada, H.
2009
- **The Role of Surface Charge and Binding Properties in Silicon-Based Field Effect Nanowire Biosensors** *Transducers 2009, Denver, CO*
Liu, Y., Dutton, R., W.
2009: 1678-1681
- **Modeling and Simulation of Orientation-Dependent Fluctuations in Nanowire Field-Effect Biosensors Using the Stochastic Linearized Poisson-Boltzmann Equation**
Heitzinger, C., Ringhofer, C., Liu, Y., Dutton, R., W.
2009
- **Lateral Ge/SiGe/Si Hetero-channel p-Type MOSFETs**
Chen, C., Y., Liu, Y., Kim, J., Dutton, R., W.
2009
- **Double-Well Field Effect Diode vs. SCR Behavior under CDM Stress in 45nm SOI Technology**
Salman, A., A., Cao, S., Beebe, S., G., Pelella, M., M., Dutton, R., W.
2008
- **Overcoming the Screen-induced Performance Limits of Nanowire Biosensors: A Simulation Study on the Effect of Electro-Diffusion Flow**
Liu, Y., Lilja, K., Heitzinger, C., Dutton, R., W.
2008
- **Progress in Biosensor and Bioelectronics Simulations: New Applications for TCAD**
Hassibi, A., Liu, Y., Dutton, R., W.
2008
- **Effect of Electrodiffusion Current Flow on Electrostatic Screening in Aqueous Pores** *J. Appl. Phys.*
Liu, Y., Sauer, J., Dutton, R., W.
2008; 8 (103)

- **An Effective Algorithm for Numerical Schrodinger Solver of Quantum Well Structures** *Journal of Computational Electronics*
Kim, J., Chen, C., -Y., Dutton, R., W.
2008; 1 (7): 1-5
- **Foreword Special Issue on Simulation and Modeling of Nanoelectronics Devices** *IEEE Trans. Electron Devices*
Sangiorgi, E., Asenov, A., Bennett, H., S., Dutton, R., W., Esseni, D., Giles, M., D.
2007; 9 (54): 2072 - 2078
- **A Circuit-Based Noise Parameter Extraction Technique for MOSFETs**
Navid, R., Lee, T., H., Dutton, R., W.
2007
- **Macro-model for post-breakdown 90nm and 130nm transistors and its applications in predicting chip-level function failure after ESD-CDM events** *45th Annual IEEE International Reliability Physics Symposium*
Chen, T. W., Ito, C., Loh, W., Wang, W., Mitra, S., Dutton, R. W.
IEEE.2007: 78-85
- **Thermal Modeling and Device Noise Properties of 3D-SOI Technology**
Chen, T., W., Chun, J., H., Lu, Y., C., Navid, R., Wang, W., Dutton, R., W.
2007
- **Electro-Thermal, Transient, Mixed-Mode 2D Simulation Study of SiC Power Thyristors Operating Under Pulsed-Power Conditions**
Hillkirk, L., M., Hefner, A., R., Dutton, R., W., Bayne, S., B., O'Brien, H.
2007
- **Gate Oxide Reliability Characterization in the 100ps Regime with Ultra-fast Transmission Line Pulsing System**
Chen, T., W., Ito, C., Maloney, T., Loh, W., Dutton, R., W.
2007
- **Simulation of p-n Junction Properties of Nanowires and Nanowire Arrays**
Hu, J., Liu, Y., Maslov, A., Ning, C, Z., Dutton, R., W., Kang, S. M.
2007
- **RF ESD Protection Strategies: Codesign vs. Low-C Protection** *Microelectronics Reliability*
Soldner, W., Streibl, M., Hodel, U., Tiebout, M., Gossner, H., Schmitt-Landsiedel, D., Dutton, R. W.
2007; 7 (47): 1008-1015
- **Physics-based Numerical Simulation for Design of High-voltage, Extremely-high Current Density SiC Power Devices**
Hillkirk, L., M., Hefner, A., R., Dutton, R., W.
2007
- **A Simple Technique for the Monte Carlo Simulation of Transport in Quantum Wells**
Kim, J., Chen, C., Y., Dutton, R., W.
2007
- **Modeling and Measurements of Electrical and Thermal Memory Effects for RF power LDMOS**
Tornblad, O., Wu, B., Dai, W., Blair, C., Ma, G., Dutton, R., W.
2007
- **Simulations of Flicker Noise in SiGe H MOS: Body Bias Dependence** *SASIMI, Sapporo, Japan*
Chen, C., Y., Liu, Y., Dutton, R., W., Sato-Iwanaga, J., Inoue, A., Sorada, H.
2006: 238-241
- **Silencer Pro: A Synthesized Compact Models-Enabled CAD Tool for Substrate Noise Analysis** *SASIMI, Nagoya, Japan*
Lan, H., MacClary, M., Mayaram, K., Fiez, T., S., Dutton, R., W.
2006
- **Modeling of Charge Trapping Induced Threshold-Voltage Instability in High-k Gate Dielectric FETs** *IEEE Electron Dev. Lett*
Liu, Y., Shanware, A., Colombo, L., Dutton, R., W.
2006; 6 (27): 489-491

- **Numerical Simulation of Field-Induced Inter-Band Tunneling Effect Transistor Using TCAD-Based Device Simulator** *64th Device Research Conference, State College, PA*
Kim, K., R., Park, B., G., Dutton, R., W.
2006: 119-120
- **Numerical Investigation of Low Frequency Noise in MOSFETs with High-k Gate Stacks** *IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Monterey, CA*
Liu, Y., Cao, S., Dutton, R., W.
2006: 99-102
- **Device Analysis of Linearity in RF Power Devices by Harmonic Balance Device Simulation**
Tornblad, O., Ma, G., Dutton, R., W.
2006
- **A Frequency-Domain VF-TLP Pulse Characterization Methodology and Its Application to CDM ESD Modeling**
Ito, C., Loh, W., Chen, T., W., Dutton, R., W.
2006
- **Erratum: "Comprehensive Study of Noise Processes in Electrode Electrolyte Interfaces" [J. Appl. Phys. 96, 1074 (2004)]** *J. Appl. Phys.*
Hassibi, A., Navid, R., Dutton, R., W., Lee, T., H.
2005; 6 (98)
- **Coupled Optical and Electronic Simulations of Electrically Pumped Photonic-Crystal-Based LEDs**
Veronis, G., Liu, Y., Suh, W., Han, M., Wang, Z., Dutton, R., W.
2005
- **Coupled Electron-Phonon Transport in Nanometer-Scale Silicon Devices** *SRC TechCon, Portland OR*
Rowlette, J., Pop, E., Sinha, S., Dutton, R., W., Goodson, K., E.
2005
- **Joule heating under quasi-ballistic transport conditions in bulk and strained silicon devices** *International Conference on Simulation of Semiconductor Processes and Devices*
Pop, E., Rowlette, J. A., DUTTON, R. W., Goodson, K. E.
JAPAN SOCIETY APPLIED PHYSICS.2005: 307-310
- **Synthesized Compact Model and Experimental Results for Substrate Noise Coupling in Lightly Doped Processes**
Lan, H., Chen, T., W., Chui, C., O., Nikaeen, P., Kim, J., W., Dutton, R., W.
2005
- **Modeling and Simulation of Jitter in Phase-Locked Loops due to Substrate Noise**
Kim, J., W., Lu, Y., C., Dutton, R., W.
2005
- **Linearity Analysis of RF LDMOS Devices Utilizing Harmonic Balance Device Simulation**
Tornblad, O., Ito, C., Rotella, F., Ma, G., Dutton, R., W.
2005
- **Electro-Thermal Simulations of Nanoscale Transistors with Optical and Acoustic Phonon Head Conduction**
Chun, J., H., Kim, B., Liu, Y., Tornblad, O., Dutton, R., W.
2005
- **Effects of Local Electric Field and Effective Tunnel Mass on the Simulation of Band-to-band Tunnel Diode Model**
Kim, K., R., Dutton, R., W.
2005
- **A New Method for Sensitivity Analysis of Photonic Crystal Devices**
Veronis, G., Dutton, R., W., Fan, S.
2005
- **Small-Signal Modeling of RF CMOS** *IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Munich, Germany*

- Jang, J., Dutton, R., W.
2004
- **Effects of Scaling on the SNR and Speed of Biosensors**
Hassibi, A., Lee, T., H., Navid, R., Dutton, R., W., Zahedi, S.
2004
 - **New Capabilities for Verilog-A Implementations of Compact Device Models** *Nanotech, Boston, MA*
Mierzwinski, M., O'Halloran, P., Troyanovsky, B., Mayaram, K., Dutton, R., W.
2004
 - **Electro-thermal comparison and performance optimization of thin-body SOI and GOI MOSFETs** *50th IEEE International Electron Devices Meeting*
Pop, E., Chui, C. O., Sinha, S., Dutton, R., Goodson, K.
IEEE.2004: 411-414
 - **Compact Modeling and Experimental Verification of Substrate Resistance in Lightly Doped Substrates**
Lan, H., Chen, T., W., Chui, C., O., Dutton, R., W.
2004
 - **Technology Limits and Compact Model for SiGe Scaled FETs** *Nanotech, Boston, MA*
Dutton, R., W., Choi, C. H.
2004
 - **Synthesized Compact Models (SCM) for Substrate Noise Coupling in Mixed-Signal Ics** *Design, Automation and Test in Europe 2004 (DATE '04), CNIT La Defence, Paris, France*
Lan, H., Dutton, R., W.
2004: 836-841
 - **Realization of Digital Noise Emulator for Characterization of Systems Exposed to Substrate Noise** *SASIMI, Kanazawa, Japan*
Lu, Y., C., Kim, J., W., Nakano, N., Colleran, D., Yue, P., Dutton, R., W.
2004
 - **Modeling of Wave Behavior of Substrate Noise Coupling for Mixed-Signal IC Design** *ISQED, San Jose, CA*
Veronis, G., Lu, Y. C., Dutton, R., W.
2004: 303-308
 - **Electro-thermal Simulations of Strained-Si MOSFETs under ESD Conditions**
Chun, J. H., Choi, C. H., Dutton, R., W.
2004
 - **Close-in Phase Noise in Electrical Oscillators**
Navid, R., Jungemann, C., Lee, T., Dutton, R., W.
2004
 - **A PMOSFET ESD Failure Caused by Localized Charge Injection**
Chun, J., H., Duvvury, C., Boselli, G., Kunz, H., Dutton, R., W.
2004
 - **Reprogrammable, Wide Tuning Range 1.6GHz CMOS VCO with Low Phase Noise Variation**
Papalias, T., A., Lee, T., T., Hajimiri, A., Dutton, R., W., Lee, T., H.
2004
 - **Synthesized Compact Models for Mixed Signal Design and Noise Analysis** *AFRA/SNDM NeoCAD Final Report*
Dutton, R., W., Kim, J., W., Lan, H., Lu, Y. C.
2004
 - **Accurate small-signal model and its parameter extraction in RF silicon MOSFETs** *IEEE MTT-S International Microwave Symposium*
Jang, J. J., Yu, Z. P., DUTTON, R. W.
IEEE.2003: 2109-2111

- **Implementation of Temperature Dependent Contact Resistance Model for the Analysis of Deep Submicron Devices under ESD**
Chun, J., H., Liu, Y., Duvvury, C., Dutton, R., W.
2003
- **A CAD-Oriented Modeling Approach of Frequency-Dependent Behavior of Substrate Noise Coupling for Mixed-Signal IC Design**
Lan, H., Yu, Z., Dutton, R., W.
2003
- **Algorithm for Evaluating Nodal Vector Quantities in Device Simulation and its Applications to Modeling Quantum Mechanical Effects in Sub-50nm MOSFETs**
Yu, Z., Yergeau, D., W., Dutton, R., W.
2003
- **Interconnect Parasitic Extraction of Resistance, Capacitance, and Inductance** *Interconnect Technology and Design for Gigascale Integration*
Qi, X., Dutton, R., W.
edited by Davis, J., Meindl, J., D.
Kluwer Academic Publishers.2003: 1
- **Implications of Gate Tunneling and Quantum Effects on Compact Modeling in the Gate-Channel Stack** *NanoTech*
Dutton, R., W., Choi, C, H.
2003
- **Detailed heat generation simulations via the Monte Carlo method** *IEEE International Conference on Simulation of Semiconductor Processes and Devices*
Pop, E., Dutton, R., Goodson, K.
IEEE.2003: 121–124
- **Hydrodynamic Modeling of RF Noise in CMOS Devices**
Jungemann, C., Neinhuis, B., Nguyen, C., D., Meinerzhagen, B., Dutton, R., W., Scholten, A., J.
2003
- **Efficient Techniques for Reducing Substrate Model Complexity in Mixed-Signal IC's**
Lan, H., Lu, Y., Nakano, N., Dutton, R., W.
2003
- **Lumped, Inductorless Oscillators: How Far Can They Go**
Navid, R., Lee, T., H., Dutton, R., W.
2003
- **Compact Modeling and Design Using Ultra-thin SOI Devices-Implications of Gate Tunneling and Quantum Effects**
Dutton, R., W., Choi, C., H.
2003
- **Circuit Impact of Gate Leakage and Thermal Modeling for Ultra-scaled MOS Devices**
Dutton, R., W., Pop, E., Choi, C, H.
2003
- **Behavioral Simulation Techniques for Substrate Noise Analysis in PLL Circuits**
Kim, J., W., Perrott, M., H., Dutton, R., W.
2003
- **Characterization of Zener-Tunneling Drain Leakage Current in High-Dose Halo Implants**
Choi, C., H., Yang, S., H., Pollack, G., Ekbote, S., Chiadambaram, P., R., Johnson, S., Dutton, R. W.
2003
- **Investigation of Thermal Breakdown Mechanism in 0.13/spl mu/m Technology ggNMOS under ESD Condition**
Hillkirk, L., M., Chun, J., Dutton, R., W.
2003
- **Hydrodynamic Simulation of RF Noise in Deep-submicron MOSFETs**
Oh, T-Y., Jungemann, C., Dutton, R., W.

2003

- **Modeling of Temperature Dependent Contact Resistance for Analysis of ESD Reliability**
Oh, K-H., Chun, J., Banerjee, K., Duvvury, C., Dutton, R., W.
2003
- **Monte Carlo Simulation of Heat Generation in Silicon Nano-Devices** *SRC TechCon, Dallas, TX*
Pop, E., Goodson, K., Dutton, R., W.
2003
- **Device Design of SiGe HBTs with Low Distortion Characteristics using Harmonic Balance Device Simulator**
Sato-Iwanaga, J., Asai, A., Takagi, T., Tanabe, M., Yu, Z., Dutton, R., W.
2003
- **Thermal Analysis of Ultra-Thin Body Device Scaling [SOI and FinFet Devices]** *IEEE International Electron Devices Meeting (IEDM) Technical Digest, Washington, D.C.*
Pop, E., Goodson, K., Dutton, R., W.
2003: 36.6.1-36.6.4
- **Analysis of Gate Bias Induced Heating Effects in Deep Submicron ESD Protection Designs** *IEEE Trans. on Device and Materials Reliability*
Oh, K., H., Duvvury, C., Banerjee, K., Dutton, R., W.
2002; 2 (2): 36-42
- **AC Analysis of Thin Gate Oxide MOS with Quantum Mechanical Corrections**
Oh, T, Y., Yu, Z., Dutton, R., W.
2002
- **Performance Improvement in Larger RF LDMOSFET Power Amplifiers**
Ito, C., Fujioka, T., Yoshida, I., Dutton, R., W.
2002
- **Hot-Carrier Energy Distribution Model and its Application to the MOSFET Substrate Current**
Lee, C., Jin, G., Lee, K., Kong, J., Lee, W., Rho, Y., Dutton, R. W.
2002
- **The Physical Phenomena Responsible for Excess Noise in Short-Channel MOS Devices**
Navid, R., Dutton, R., W.
2002
- **Investigation of Gate to Contact Spacing Effect on ESD Robustness of Salicided Deep Submicron Single Finger NMOS Transistors**
Oh, K-H., Duvvury, C., Banerjee, K., Dutton, R., W.
2002
- **Non-Uniform Conduction Induced Reverse Channel Length Dependence of ESD Reliability for Silicided NMOS Transistors** *IEEE International Electron Devices Meeting (IEDM) Technical Digest, San Francisco, CA*
Oh, K, H., Banerjee, K., Duvvury, C., Dutton, R., W.
2002: 341-344
- **An OO-PDE Solver for TCAD Apps** *IEEE Potentials*
Yergeau, D., W., Dutton, R., W., Goosens, R., J. G.
2002; 2 (21): 25-29
- **Two-dimensional polysilicon quantum-mechanical effects in double-gate SOI** *IEEE International Electron Devices Meeting*
Choi, C. H., Yu, Z. P., DUTTON, R. W.
IEEE.2002: 723-726
- **Series Resistance Calculation for Source/Drain Extension Using 2-D Device Simulation** *IEEE Trans. Electron Devices*
Kwong, M., Y., Choi, C., -H., Kasnavi, R., Griffin, P., Dutton, R., W.
2002; 7 (49): 1219-1226
- **Accurate Model of Metal-Insulator-Semiconductor Interconnects**

-
- Wang, G., Qi, X., Yu, Z., Dutton, R., W.
2002
- **What Can Computer Aided Engineering Do for the SOC Era?**
Masuda, H., Orlowski, M., Dutton, R., W., Fukuma, M., Lee, S., W., Schoenmaker, W.
2002
 - **Nanoscale Heat Generation in Silicon via the Monte Carlo Method**
Pop, E., Sinha, S., Dutton, R., W., Goodson, K.
2002
 - **Analytical Analysis of Short-Channel Effects in MOSFETs for sub-100nm Technology** *Electronics Letters*
Park, J. S., Lee, S. Y., Shin, H., Dutton, R., W.
2002; 20 (38): 1222-1223
 - **RF LDMOS characterization and its compact modeling** *IEEE MTT-S International Microwave Symposium*
Jang, J. J., Tornblad, O., Arnborg, T., Chen, Q., Banerjee, K., Yu, Z. P., DUTTON, R. W.
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 - **Localized Heating Effects and Scaling of Sub-0.18 Micron CMOS Devices**
Pop, E., Banerjee, K., Sverdrup, P., Dutton, R., W., Goodson, K.
2001
 - **High Frequency Characterization and Modeling of VLSI On-Chip Interconnects**
Qi, X., Kleveland, B., Wang, G., Yu, Z., Wong, S., S., Dutton, R., W.
2001
 - **A Fast Analytical Technique for Estimating the Bounds of On-Chip Clock Wire Inductance**
Lu, Y., Banerjee, K., Celik, M., Dutton, R., W.
2001
 - **Non-uniform Bipolar Conduction in Single Finger NMOS Transistors and Implications for Deep Submicron ESD Design**
Oh, K-H., Duvvury, C., Salling, C., Banerjee, K., Dutton, R., W.
2001
 - **Quantum Transport Model for sub-100nm CMOS Devices**
Yu, Z., Yergeau, D., W., Dutton, R., W., Svizhenko, A., Anantram, M., P.
2001
 - **Analysis and Design of ESD Protection Circuits for High-Frequency/RF Applications**
Ito, C., Banerjee, K., Dutton, R., W.
2001
 - **Gate Bias Induced Heating Effect and Implications for the Design of Deep Submicron ESD Protection**
Oh, K, H., Duvvury, C., Banerjee, K., Dutton, R., W.
2001
 - **Density Functional Theory Study of Hf and Zr Aluminates as High-k Gate Dielectrics**
Haverty, M., Kawamoto, A., Jun, G., Cho, K., Dutton, R., W.
2001
 - **Impact of Gate Tunneling Current in Scaled MOS on Circuit Performance: A Simulation Study**
Choi, C-H., Yu, Z., Dutton, R., W.
2001
 - **Design Methodology for Power-Constrained Low Noise RF Circuits**
Goo, J-S., Ahn, H, T., Ladwig, D., J., Yu, Z., Lee, T., H., Dutton, R., W.
2001
 - **Fast Placement-Dependent Full Chip Thermal Simulation**
Yu, Z., Yergeau, D., Dutton, R., W., Nakagawa, S., Deeney, J.

2001

- **Analysis and Optimization of Distributed ESD Protection Circuits for High-Speed Mixed Signal and RF Applications**
Ito, C., Banerjee, K., Dutton, R., W.
2001
- **Impact of substrate resistance on drain current noise in MOSFETs** *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 01)*
Goo, J. S., Donati, S., Choi, C. H., Yu, Z. P., Lee, T. H., DUTTON, R. W.
SPRINGER-VERLAG WIEN.2001: 182–185
- **Macroscopic quantum carrier transport modeling** *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 01)*
Yu, Z. P., DUTTON, R. W., YERGEAU, D. W., Ancona, M. G.
SPRINGER-VERLAG WIEN.2001: 1–9
- **Large signal analysis of on-chip interconnects using transport based approach** *5th International Symposium on Antennas, Propagation and EM Theory (ISAPE 2000)*
Wang, G. F., Qi, X. N., Yu, Z. P., DUTTON, R. W., Rafferty, C. S.
IEEE.2000: 309–312
- **Qualification of Hemodynamics in the Human Abdominal Aorta using Level Set Based Vascular Modeling**
Wang, K., Dutton, R., W., Taylor, C.
2000
- **Advanced Electro-Thermal Modeling and Simulation Techniques for Deep Sub-Micron Devices**
Sverdrup, P., G., Sinha, S., Pop, E., Tornblad, O., Dutton, R., W., Goodson, K., E.
2000
- **Well-tempered MOSFETs: 1D Versus 2D Quantum Analysis**
Abramo, A., Selmi, L., Yu, Z., Dutton, R., W.
2000
- **Atomic Scale Effects of Zirconium and Hafnium Incorporation at a Model Silicon/silicate Interface by First Principles Calculations**
Kawamoto, A., Jameson, J., Griffin, P., B., Cho, K., Dutton, R., W.
2000
- **Internet Based Modeling of Micro-Electro-Mechanical Systems**
Wilson, X., M., Yergeau, D., W., Dutton, R., W.
2000
- **Guidelines for the power constrained design of a CMOS tuned LNA** *International Conference on Simulation of Semiconductor Processes and Devices*
Goo, J. S., Oh, K. H., Choi, C. H., Yu, Z. P., Lee, T. H., DUTTON, R. W.
IEEE.2000: 269–272
- **Sub-continuum thermal simulations of deep sub-micron devices under ESD conditions** *International Conference on Simulation of Semiconductor Processes and Devices*
Sverdrup, P. G., Banerjee, K., Dai, C. H., Shih, W. K., DUTTON, R. W., Goodson, K. E.
IEEE.2000: 54–57
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