Stanford

Robert Dutton

Robert and Barbara Kleist Professor in the School of Engineering, Emeritus

Electrical Engineering

Bio

BIO

Dutton's group develops and applies computer aids to process modeling and device analysis. His circuit design activities emphasize layout-related issues of parameter extraction and electrical behavior for devices that affect system performance. Activities include primarily silicon technology modeling both for digital and analog circuits, including OE/RF applications. New emerging area now includes bio-sensors and the development of computer-aided bio-sensor design.

ACADEMIC APPOINTMENTS

- Emeritus Faculty, Acad Council, Electrical Engineering

HONORS AND AWARDS

- J.J. Ebers Award, Institute of Electrical and Electronics Engineers (1987)
- Jack A. Morton Award, Institute of Electrical and Electronics Engineers (1996)
- SIA University Researcher Award, Semiconductor Industry Association (2000)
- Phil Kaufman Award, Electronic Design Automation Consortium (2006)

BOARDS, ADVISORY COMMITTEES, PROFESSIONAL ORGANIZATIONS

- member, National Academy of Engineering (1991 - present)
- Member, Semiconductor Industries Association (2005 - present)

PROFESSIONAL EDUCATION

- PhD, UC Berkeley (1970)

LINKS

- http://www-tcad.stanford.edu/tcad/bios/dutton.html: http://www-tcad.stanford.edu/tcad/bios/dutton.html

Teaching

COURSES

2020-21

- The Electrical Engineering Profession: EE 100 (Aut)

2019-20

- The Electrical Engineering Profession: EE 100 (Aut)

2018-19

- Analog Communications Design Laboratory: EE 133, EE 233 (Win)
- The Electrical Engineering Profession: EE 100 (Aut)

Publications

PUBLICATIONS

- **Proc. of the ICSSDP** *Simulation of Multilayer Structures for VLSI Using the SUPREM-III Process Simulation Program*
  Hansen, S., E., Shott, J., D., Fahey, P., M., Plummer, J., D., Dutton, R., W., K.
  edited by R.J., Board, D.
  Pineridge Press.
- **Simulation of Integrated Circuits Design** *Process and Device Modeling for Integrated Circuit Design*
  Antoniadis, D., A., Dutton, R., W.
- **New Challenges in Device Design for Integrated Electronic Systems**
  Dutton, R., W., Yu, Z.
- **Analysis of Advanced Devices Using Industry-Networked Technology CAD (ALADDIN-CAD)** *Final Report, California Competitive Technology Program (CompTech Grant # C90-072).*
  Dutton, R., W.
- **Workload Dependent NBTI and PBTI Analysis for a Sub-45nm Commercial Microprocessor** *IEEE IRPS, Anaheim, CA*
  Mintarno, E., Chandra, V., Pietromonaco, D., Aitken, R., Dutton, R., W.
  2013: 3A.1.1-3A.1.6
- **Applications of NanoNewton Dielectrophoretic Forces using Atomic Layer Deposited Oxides for Microfluidic Sample Preparation and Proteomics**
  Emaminejad, S., Javanmare, M., Gupta, C., Dutton, R., W., Davis, R., W., Howe, R., T.
  2013
- **Smart surfaces: Use of electrokinetics for selective modulation of biomolecular affinities**
  Emaminejad, S., Javanmard, M., Dutton, R., W., Davis, R., W.
  2012
- **Efficient Control of DNA Transport in Nanopore-based Nanofluidic Transistors**
  Paik, K., H., Liu, Y., Tabard-Cossa, V., Huber, D., Provine, J., Howe, R., Dutton, R. W.
  2011
- **An Electronic Microfluidic Switch using Dielectrophoresis for Control of Microparticles**
  Javanmard, M., Emaminejad, S., Dutton, R., W., Davis, R.
  2011
- **Smart Surfaces: Use of Electrokinetics for Selective Modulation of Biomolecular Affinities** *MRS Fall Meeting, Boston, MA*
  Emaminejad, S., Javanmard, M., Dutton, R., W., Davis, R., W.
  2011; 1414
- **Field Effect Resistor, a Single-Device-at-Pad Solution for ESD Protection in Deeply Scaled SOI Technology**
  Cao, S., Salman, A., A., Chun, J., H., Beebe, S., G., Pelella, M., M., Dutton, R., W.
  2010
- **Modeling and RF Analysis of Silicon Inter-band Tunnel Diode with THz Cut-off Frequency**
  Kim, K., R., Kang, I., M., Dutton, R., W.
  2010
- **Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering**
  Cao, S., Chun, J., H., Choi, E., Beebe, S., Anderson, W., Dutton, R., W.
  2010
- **Optimized Self-Tuning for Circuit Aging**

Mintarno, E., Skaf, J., Zheng, R., Velamala, J., Cao, Y., Boyd, S., Dutton, R. W.
2010

- **Electrical Modulation of Ion Concentration in Dual-Gated Nanochannels**
  Liu, Y., Ran, Q., Dutton, R., W.
  2010
- **ESD Design Challenges and Strategies in Deeply-Scaled Integrated Circuits**
  Cao, S., Chen, T., W., Beebe, S., G., Dutton, R., W.
  2009
- **Field Effect Diode for Effective CDM ESD Protection in 45nm SOI Technology**
  Cao, S., Beebe, S., G., Salman, A., A., Pelella, M., M., Chun, J, H., Dutton, R., W.
  2009
- **Numerical Flicker Noise Model for Dual Channel FETs**
  Chen, C., Y., Liu, Y., Dutton, R., W., Sato-Iwanaga, J., Inoue, A., Sorada, H.
  2009
- **The Role of Surface Charge and Binding Properties in Silicon-Based Field Effect Nanowire Biosensors** *Transducers 2009, Denver, CO*
  Liu, Y., Dutton, R., W.
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- **Modeling and Simulation of Orientation-Dependent Fluctuations in Nanowire Field-Effect Biosensors Using the Stochastic Linearized Poisson-Boltzmann Equation**
  Heitzinger, C., Ringhofer, C., Liu, Y., Dutton, R., W.
  2009
- **Lateral Ge/SiGe/Si Hetero-channel p-Type MOSFETs**
  Chen, C., Y., Liu, Y., Kim, J., Dutton, R., W.
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- **Double-Well Field Effect Diode vs. SCR Behavior under CDM Stress in 45nm SOI Technology**
  Salman, A., A., Cao, S., Beebe, S., G., Pelella, M., M., Dutton, R., W.
  2008
- **Overcoming the Screen-induced Performance Limits of Nanowire Biosensors: A Simulation Study on the Effect of Electro-Diffusion Flow**
  Liu, Y., Lilja, K., Heitzinger, C., Dutton, R., W.
  2008
- **Progress in Biosensor and Bioelectronics Simulations: New Applications for TCAD**
  Hassibi, A., Liu, Y., Dutton, R., W.
  2008
- **Effect of Electrodiffusion Current Flow on Electrostatic Screening in Aqueous Pores** *J. Appl. Phys.*
  Liu, Y., Sauer, J., Dutton, R., W.
  2008; 8 (103)
- **An Effective Algorithm for Numerical Schrodinger Solver of Quantum Well Structures** *Journal of Computational Electronics*
  Kim, J., Chen, C., -Y., Dutton, R., W.
  2008; 1 (7): 1-5
- **Foreword Special Issue on Simulation and Modeling of Nanoelectronics Devices** *IEEE Trans. Electron Devices*
  Sangiorgi, E., Asenov, A., Bennett, H., S., Dutton, R., W., Esseni, D., Giles, M., D.
  2007; 9 (54): 2072 - 2078
- **A Circuit-Based Noise Parameter Extraction Technique for MOSFETs**
  Navid, R., Lee, T., H., Dutton, R., W.
  2007

- **Macro-model for post-breakdown 90nm and 130nm transistors and its applications in predicting chip-level function failure after ESD-CDM events** *45th Annual IEEE International Reliability Physics Symposium*
  Chen, T. W., Ito, C., Loh, W., Wang, W., Mitra, S., Duttona, R. W.
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- **Thermal Modeling and Device Noise Properties of 3D-SOI Technology**
  Chen, T., W., Chun, J., H., Lu, Y., C., Navid, R., Wang, W., Dutton, R., W.
  2007
- **Electro-Thermal, Transient, Mixed-Mode 2D Simulation Study of SiC Power Thyristors Operating Under Pulsed-Power Conditions**
  Hillkirk, L., M., Hefner, A., R., Dutton, R., W., Bayne, S., B., O'Brien, H.
  2007
- **Gate Oxide Reliability Characterization in the 100ps Regime with Ultra-fast Transmission Line Pulsing System**
  Chen, T., W., Ito, C., Maloney, T., Loh, W., Dutton, R., W.
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- **Simulation of p-n Junction Properties of Nanowires and Nanowire Arrays**
  Hu, J., Liu, Y., Maslov, A., Ning, C, Z., Dutton, R., W., Kang, S. M.
  2007
- **RF ESD Protection Strategies: Codesign vs. Low-C Protection** *Microelectronics Reliability*
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  Hillkirk, L., M., Hefner, A., R., Dutton, R., W.
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- **A Simple Technique for the Monte Carlo Simulation of Transport in Quantum Wells**
  Kim, J., Chen, C., Y., Dutton, R., W.
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- **Modeling and Measurements of Electrical and Thermal Memory Effects for RF power LDMOS**
  Tornblad, O., Wu, B., Dai, W., Blair, C., Ma, G., Dutton, R., W.
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- **Simulations of Flicker Noise in SiGe HMOS: Body Bias Dependence** *SASIMI, Sapporo, Japan*
  Chen, C., Y., Liu, Y., Dutton, R., W., Sato-Iwanaga, J., Inoue, A., Sorada, H.
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- **Numerical Simulation of Field-Induced Inter-Band Tunneling Effect Transistor Using TCAD-Based Device Simulator** *64th Device Research Conference, State College, PA*
  Kim, K., R., Park, B., G., Dutton, R., W.
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- **Numerical Investigation of Low Frequency Noise in MOSFETs with High-k Gate Stacks** *IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Monterey, CA*
  Liu, Y., Cao, S., Dutton, R., W.
  2006: 99-102
- **Device Analysis of Linearity in RF Power Devices by Harmonic Balance Device Simulation**

Tornblad, O., Ma, G., Dutton, R., W.
2006

- **A Frequency-Domain VFTLP Pulse Characterization Methodology and Its Application to CDM ESD Modeling**
  Ito, C., Loh, W., Chen, T., W., Dutton, R., W.
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- **Erratum: "Comprehensive Study of Noise Processes in Electrode Electrolyte Interfaces" [J. Appl. Phys. 96, 1074 (2004)]** *J. Appl. Phys.*
  Hassibi, A., Navid, R., Dutton, R., W., Lee, T., H.
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  Veronis, G., Liu, Y., Suh, W., Han, M., Wang, Z., Dutton, R., W.
  2005
- **Coupled Electron-Phonon Transport in Nanometer-Scale Silicon Devices** *SRC TechCon, Portland OR*
  Rowlette, J., Pop, E., Sinha, S., Dutton, R., W., Goodson, K., E.
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- **Joule heating under quasi-ballistic transport conditions in bulk and strained silicon devices** *International Conference on Simulation of Semiconductor Processes and Devices*
  Pop, E., Rowlette, J. A., DUTTON, R. W., Goodson, K. E.
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- **Synthesized Compact Model and Experimental Results for Substrate Noise Coupling in Lightly Doped Processes**
  Lan, H., Chen, T., W., Chui, C., O., Nikaeen, P., Kim, J., W., Dutton, R., W.
  2005
- **Modeling and Simulation of Jitter in Phase-Locked Loops due to Substrate Noise**
  Kim, J., W., Lu, Y., C., Dutton, R., W.
  2005
- **Linearity Analysis of RF LDMOS Devices Utilizing Harmonic Balance Device Simulation**
  Tornblad, O., Ito, C., Rotella, F., Ma, G., Dutton, R., W.
  2005
- **Electro-Thermal Simulations of Nanoscale Transistors with Optical and Acoustic Phonon Head Conduction**
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  Veronis, G., Dutton, R., W., Fan, S.
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- **Small-Signal Modeling of RF CMOS** *IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Munich, Germany*
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- **Technology Limits and Compact Model for SiGe Scaled FETs** *Nanotech, Boston, MA*
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- **Synthesized Compact Models (SCM) for Substrate Noise Coupling in Mixed-Signal Ics** *Design, Automation and Test in Europe 2004 (DATE '04), CNIT La Defence, Paris, France*
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- **Modeling of Wave Behavior of Substrate Noise Coupling for Mixed-Signal IC Design** *ISQED, San Jose, CA*
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- **Electro-thermal Simulations of Strained-Si MOSFETs under ESD Conditions**
  Chun, J, H., Choi, C, H., Dutton, R., W.
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- **Close-in Phase Noise in Electrical Oscillators**
  Navid, R., Jungemann, C., Lee, T., Dutton, R., W.
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- **A PMOSFET ESD Failure Caused by Localized Charge Injection**
  Chun, J., H., Duvvury, C., Boselli, G., Kunz, H., Dutton, R., W.
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- **Synthesized Compact Models for Mixed Signal Design and Noise Analysis** *AFRA/SNDM NeoCAD Final Report*
  Dutton, R., W., Kim, J., W., Lan, H., Lu, Y, C.
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- **Accurate small-signal model and its parameter extraction in RF silicon MOSFETs** *IEEE MTT-S International Microwave Symposium*
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- **Implementation of Temperature Dependent Contact Resistance Model for the Analysis of Deep Submicron Devices under ESD**
  Chun, J., H., Liu, Y., Duvvury, C., Dutton, R., W.
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- **A CAD-Oriented Modeling Approach of Frequency-Dependent Behavior of Substrate Noise Coupling for Mixed-Signal IC Design**
  Lan, H., Yu, Z., Dutton, R., W.
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- **Algorithm for Evaluating Nodal Vector Quantities in Device Simulation and its Applications to Modeling Quantum Mechanical Effects in Sub-50nm MOSFETs**
  Yu, Z., Yergeau, D., W., Dutton, R., W.

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- **Interconnect Parasitic Extraction of Resistance, Capacitance, and Inductance** *Interconnect Technology and Design for Gigascale Integration*
  Qi, X., Dutton, R., W.
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  2003
- **Efficient Techniques for Reducing Substrate Model Complexity in Mixed-Signal IC's**
  Lan, H., Lu, Y., Nakano, N., Dutton, R., W.
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- **Lumped, Inductorless Oscillators: How Far Can They Go**
  Navid, R., Lee, T., H., Dutton, R., W.
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- **Compact Modeling and Design Using Ultra-thin SOI Devices-Implications of Gate Tunneling and Quantum Effects**
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- **Circuit Impact of Gate Leakage and Thermal Modeling for Ultra-scaled MOS Devices**
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- **Behavioral Simulation Techniques for Substrate Noise Analysis in PLL Circuits**
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- **Investigation of Thermal Breakdown Mechanism in 0.13/spl mu/m Technology ggNMOS under ESD Condition**
  Hillkirk, L., M., Chun, J., Dutton, R., W.
  2003
- **Hydrodynamic Simulation of RF Noise in Deep-submicron MOSFETs**
  Oh, T-Y., Jungemann, C., Dutton, R., W.
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- **Modeling of Temperature Dependent Contact Resistance for Analysis of ESD Reliability**
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2003

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  Oh, T, Y., Yu, Z., Dutton, R., W.
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  2002
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  2002
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  Pop, E., Banerjee, K., Sverdrup, P., Dutton, R., W., Goodson, K.
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- **High Frequency Characterization and Modeling of VLSI On-Chip Interconnects**
  Qi, X., Kleveland, B., Wang, G., Yu, Z., Wong, S., S., Dutton, R., W.
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- **A Fast Analytical Technique for Estimating the Bounds of On-Chip Clock Wire Inductance**
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- **Non-uniform Bipolar Conduction in Single Finger NMOS Transistors and Implications for Deep Submicron ESD Design**
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- **Fast Placement-Dependent Full Chip Thermal Simulation**
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  Ito, C., Banerjee, K., Dutton, R., W.
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  Goo, J. S., Donati, S., Choi, C. H., Yu, Z. P., Lee, T. H., DUTTON, R. W.
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  Abramo, A., Selmi, L., Yu, Z., Dutton, R., W.
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- **Atomic Scale Effects of Zirconium and Hafnium Incorporation at a Model Silicon/silicate Interface by First Principles Calculations**
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