



Subhasish Mitra

William E. Ayer Professor of Electrical Engineering and Professor of Computer Science

CONTACT INFORMATION

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Bio

BIO

Subhasish Mitra holds the William E. Ayer Endowed Chair Professorship in the Departments of Electrical Engineering and Computer Science at Stanford University. He directs the Stanford Robust Systems Group, serves on the leadership team of the Microelectronics Commons AI Hardware Hub funded by the US CHIPS and Science Act, leads the Computation Focus Area of the Stanford SystemX Alliance, and is the Associate Chair (Faculty Affairs) of Computer Science. His research ranges across Robust Computing, NanoSystems, Electronic Design Automation (EDA), and Neurosciences. Results from his research group have influenced almost every contemporary electronic system and have inspired significant government and research initiatives in multiple countries. He has held several international academic appointments — the Carnot Chair of Excellence in NanoSystems at CEA-LETI in France, Invited Professor at EPFL in Switzerland, and Visiting Professor at the University of Tokyo in Japan. Prof. Mitra also has consulted for major technology companies including AMD (Xilinx), Cisco, Google, Intel, Merck (EMD Electronics), and Samsung.

In the field of Robust Computing, he has created many key approaches for circuit failure prediction, CASP on-line diagnostics, QED system validation, soft error resilience, and X-Compact test compression. Their adoption by industry is growing rapidly, in markets ranging from cloud computing to automotive systems, under various names (Silicon Lifecycle Management, Predictive Health Monitoring, In-System Test Architecture, In-field Scan, In-fleet Scan). His X-Compact approach has proven essential to cost-effective manufacturing and high-quality testing of almost all 21st century systems. X-Compact and its derivatives enabled billions of dollars of cost savings across the industry.

In the field of NanoSystems, with his students and collaborators, he demonstrated several firsts: the first NanoSystems hardware among all beyond-silicon nanotechnologies for energy-efficient computing (the carbon nanotube computer), the first 3D NanoSystem with computation immersed in data storage, the first published end-to-end computing systems using resistive memories (Resistive RAM-based non-volatile computing systems delivering 10-fold energy efficiency versus embedded flash), and the first monolithic 3D integration combining heterogeneous logic and memory technologies in silicon foundry. These received wide recognition: cover of NATURE, several Highlights to the US Congress, and highlight as "important scientific breakthrough" by news organizations worldwide.

Prof. Mitra's honors include the Harry H. Goode Memorial Award (by IEEE Computer Society for outstanding contributions in the information processing field), Newton Technical Impact Award in EDA (test-of-time honor by ACM SIGDA and IEEE CEDA), the University Researcher Award (by Semiconductor Industry Association and Semiconductor Research Corporation to recognize lifetime research contributions), the EDAA Achievement Award (by European Design and Automation Association, for outstanding lifetime contributions to electronic design, automation and testing), the Intel Achievement Award (Intel's highest honor), and the Distinguished Alumnus Award from the Indian Institute of Technology, Kharagpur. He and his students have published over 15 award-winning papers across 5 topic areas (technology, circuits, EDA, test, verification) at major venues including the Design Automation Conference, International Electron Devices Meeting, International Solid-State Circuits Conference, International Test Conference, Symposia on VLSI Technology/VLSI Circuits, and Formal Methods in Computer-Aided Design. Stanford undergraduates have honored him several times "for being important to them." He is a Fellow of the Association for Computing Machinery (ACM) and the Institute of Electrical and Electronics Engineers (IEEE), and a Foreign Member of Academia Europaea.

ACADEMIC APPOINTMENTS

- Professor, Electrical Engineering
- Professor, Computer Science
- Member, Bio-X
- Member, Wu Tsai Human Performance Alliance
- Member, Wu Tsai Neurosciences Institute

ADMINISTRATIVE APPOINTMENTS

- Associate Chair, Faculty Affairs, Department of Computer Science, Stanford University, (2021- present)

HONORS AND AWARDS

- Achievement Award, lifetime honor for outstanding contributions to design/design automation/testing, European Design and Automation Association (EDAA) (2025)
- Roger A. Haken Best Student Paper Award, IEEE International Electron Devices Meeting (with Stanford advisee) (2024)
- Top Picks in Hardware Security, IEEE (2024)
- Best Student Paper Award, Symposium on VLSI Technology (with Stanford advisees) (2023)
- Top Picks in Test and Reliability, IEEE (2023)
- William E. Ayer Endowed Chair Professorship, Stanford University (2023)
- Distinguished Alumnus Award, Indian Institute of Technology, Kharagpur (2022)
- Harry H. Goode Memorial Award, IEEE Computer Society (2022)
- Best Student Paper Award, Symposium on VLSI Circuits (with Stanford advisees) (2021)
- Foreign Member, Academia Europaea (2021)
- University Researcher Award for lifetime research contributions to the U.S. semiconductor industry, Jointly by Semiconductor Industry Association (SIA) and Semiconductor Research Corporation (SRC) (2021)
- Honorable Mention Paper, Formal Methods in Computer-Aided Design (2020)
- Humboldt Prize (Humboldt Research Award), Alexander von Humboldt Foundation, Germany (2019)
- Faculty Research Award, Google (2018)
- Ten Year Retrospective Most Influential Paper Award, IEEE International Conference on Computer-Aided Design (2018)
- Carnot Chair of Excellence in NanoSystems, CEA-LETI, Grenoble, France (2017-2020)
- Best of SELSE, IEEE International Conference on Dependable Systems and Networks (2016)
- Special recognition for carbon nanotube research, SEMI, the global microelectronics industry association (2016)

- Best Paper Award, IEEE International Test Conference (2015)
- Technical Excellence Award, Semiconductor Research Corporation (SRC) (2015)
- A. Richard Newton Technical Impact Award in Electronic Design Automation (test of time honor), ACM SIGDA & IEEE CEDA (2014)
- Fellow, Association for Computing Machinery (ACM) (2014)
- Fellow, Institute of Electrical and Electronics Engineers (IEEE) (2013)
- Jack Raper Award for Outstanding Technology Directions Paper, IEEE International Solid-State Circuits Conference (2013)
- Kavli Foundation Fellow, United States National Academy of Sciences (2013)
- World Economic Forum Young Scientist, World Economic Forum (2013)
- Chambers Faculty Scholar, Stanford School of Engineering (2011)
- Best Paper Award, IEEE VLSI Test Symposium (2010)
- Best Student Paper Award, IEEE International Test Conference (with Stanford advsees) (2010)
- Research Highlight, Communications of the ACM (2010)
- Honored by graduating seniors as a Stanford professor who had been important to them, Stanford University School of Engineering (2009-2021)
- Invited Participant, National Academy of Engineering, US Frontiers of Engineering Symposium (2009)
- Okawa Foundation Research Grant, Okawa Foundation for Information and Telecommunications, Japan (2009)
- Best Paper Award, ACM/IEEE Design Automation Conference (2008)
- Best Student Paper Award, Symposium on VLSI Technology (with Stanford advisees) (2008)
- Outstanding New Faculty Award, ACM SIGDA (2008)
- Presidential Early Career Award for Scientists and Engineers (PECASE), The White House, the United States government (2008)
- IBM Faculty Award, IBM (2006, 2007, 2008)
- Terman Fellow, Stanford University (2006)
- Best Paper Award, Intel Design and Test Technology Conference (2005)
- Divisional Recognition award (for Breakthrough Soft Error Protection Technology), Intel Corporation (2005)
- Donald O. Pederson Outstanding Paper Award, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (2005)
- Inaugural S. Seshu Scholar Lecturer, Coordinated Science Laboratory, University of Illinois at Urbana-Champaign (2005)
- Intel Achievement Award, Intel's highest corporate honor, Intel Corporation (For the development and deployment of a breakthrough test compression technology) (2004)
- Divisional Recognition award, Intel Corporation (For Development and Proliferation of Industry Leading Response Compactor Design) (2002)
- Silver medal recipient for highest rank among all M. Tech students, Indian Institute of Technology, Kharagpur (1996)
- Cadence Fellowship, Indian Institute of Technology, Kharagpur (1994-1996)
- Gold medals for Rank 1 in engineering during all four years of undergraduate study, Jadavpur University, India (1994)

PROGRAM AFFILIATIONS

- Stanford SystemX Alliance

LINKS

- <https://rsg.stanford.edu/>: <https://rsg.stanford.edu/>

Publications

PUBLICATIONS

- **CLEAR Cross-Layer Resilience: A Retrospective** *IEEE DESIGN & TEST*

- Cheng, E., Cho, H., Mirkhani, S., Szafaryn, L., Abraham, J., Bose, P., Cher, C., Lilja, K., Skadron, K., Stan, M., Mitra, S.
2025; 42 (3): 74-85
- **Monolithic 3-D Integration of Diverse Memories: Resistive Switching (RRAM) and Gain Cell (GC) Memory Integrated on Si CMOS** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Liu, S., Radway, R. M., Wang, X., Moro, F., Nodin, J., Jana, K., Yan, L., Du, S., Upton, L. R., Chen, W., Kang, J., Chen, J., Li, et al
2025
 - **Three-Independent-Gate Transistors: The Swiss Army Knife of Devices [Special Section on 2025 IEEE Kirchhoff Award]** *IEEE CIRCUITS AND SYSTEMS MAGAZINE*
Cadareanu, P., Mitra, S., Amaru, L., Gaillardon, P.
2025; 25 (2): 17-22
 - **Omni 3D: BEOL-Compatible 3-D Logic With Omnipresent Power, Signal, and Clock** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Choi, S., Gilardi, C., Gutwin, P., Radway, R. M., Srimani, T., Mitra, S.
2025; 72 (4): 2038-2045
 - **MINOTAUR: A Posit-Based 0.42-0.50-TOPS/W Edge Transformer Inference and Training Accelerator** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
Prabhu, K., Radway, R. M., Yu, J., Bartolone, K., Giordano, M., Peddinghaus, F., Urman, Y., Khwa, W., Chih, Y., Chang, M., Mitra, S., Raina, P.
2025; 60 (4): 1311-1323
 - **Understanding responses to multi-electrode epiretinal stimulation using a biophysical model.** *Journal of neural engineering*
Vilkhu, R., Vasireddy, P., Kish, K. E., Gogliettino, A. R., Lotlikar, A., Hottowy, P., Dabrowski, W., Sher, A., Litke, A. M., Mitra, S., Chichilnisky, E. J.
2024
 - **VLSI Test and Trust Roundtable** *IEEE DESIGN & TEST*
Karri, R., Rajski, J., Aitken, R., Mitra, S., Tehranipoor, M. M.
2024; 41 (6): 84-94
 - **Precise control of neural activity using dynamically optimized electrical stimulation.** *eLife*
Shah, N. P., Phillips, A. J., Madugula, S., Lotlikar, A., Gogliettino, A. R., Hays, M. R., Grosberg, L., Brown, J., Dusi, A., Tandon, P., Hottowy, P., Dabrowski, W., Sher, et al
2024; 13
 - **Lossless Phonon Transition Through GaN-Diamond and Si-Diamond Interfaces** *ADVANCED ELECTRONIC MATERIALS*
Malakoutian, M., Woo, K., Rich, D., Mandia, R., Zheng, X., Kasperovich, A., Saraswat, D., Soman, R., Jo, Y., Pfeifer, T., Hwang, T., Aller, H., Kim, et al
2024
 - **Future Design Direction for SRAM Data Array: Hierarchical Subarray With Active Interconnect** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS*
Liu, H., Gilardi, C., Salahuddin, S. M., Pei, Z., Schuddinck, P., Xiang, Y., Weckx, P., Hellings, G., Bardou, M., Ryckaert, J., Pan, C., Mitra, S., Catthoor, et al
2024
 - **EMBER: Efficient Multiple-Bits-Per-Cell Embedded RRAM Macro for High-Density Digital Storage** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
Levy, A., Upton, L. R., Scott, M. D., Rich, D., Khwa, W., Chih, Y., Chang, M., Mitra, S., Murmann, B., Raina, P.
2024
 - **Hybrid 2T nMOS/pMOS Gain Cell Memory With Indium-Tin-Oxide and Carbon Nanotube MOSFETs for Counteracting Capacitive Coupling** *IEEE ELECTRON DEVICE LETTERS*
Liu, S., Li, S., Lin, Q., Jana, K., Mitra, S., Wong, H., Toprasertpong, K.
2024; 45 (2): 188-191
 - **Faulty Function Extraction for Defective Circuits**
Nigh, C., Purdy, R., Li, W., Mitra, S., Blanton, R. D., IEEE
IEEE.2024
 - **Efficient Ultra-Dense 3D IC Power Delivery and Cooling Using 3D Thermal Scaffolding**

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- Rich, D., Srimani, T., Malakoutian, M., Chowdhury, S., Mitra, S., ACM ASSOC COMPUTING MACHINERY.2024
- **Cooling future system-on-chips with diamond inter-tiers** *CELL REPORTS PHYSICAL SCIENCE*
Malakoutian, M., Kasperovich, A., Rich, D., Woo, K., Perez, C., Soman, R., Saraswat, D., Kim, J., Noshin, M., Chen, M., Vaziri, S., Bao, X., Shih, et al 2023; 4 (12)
 - **Band-to-Band Tunneling Leakage Current Characterization and Projection in Carbon Nanotube Transistors.** *ACS nano*
Lin, Q., Gilardi, C., Su, S. K., Zhang, Z., Chen, E., Bandaru, P., Kummel, A., Radu, I., Mitra, S., Pitner, G., Wong, H. P. 2023
 - **Effect of Back-Gate Dielectric on Indium Tin Oxide (ITO) Transistor Performance and Stability** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Daus, A., Hoang, L., Gilardi, C., Wahid, S., Kwon, J., Qin, S., Ko, J., Islam, M., Kumar, A., Neilson, K. M., Saraswat, K. C., Mitra, S., Wong, et al 2023; 70 (11): 5685-5689
 - **Micro/Nano Circuits and Systems Design and Design Automation: Challenges and Opportunities** *PROCEEDINGS OF THE IEEE*
Cauwenberghs, G., Cong, J., Hu, X., Joshi, S., Mitra, S., Porod, W., Wong, H. 2023; 111 (6): 561-574
 - **An Exhaustive Approach to Detecting Transient Execution Side Channels in RTL Designs of Processors** *IEEE TRANSACTIONS ON COMPUTERS*
Fadiheh, M., Wezel, A., Mueller, J., Bormann, J., Ray, S., Fung, J. M., Mitra, S., Stoffel, D., Kunz, W. 2023; 72 (1): 222-235
 - **PBA: Percentile-Based Level Allocation for Multiple-Bits-Per-Cell RRAM**
Wei, A., Levy, A., Yi, P., Radway, R. M., Raina, P., Mitra, S., Achour, S., IEEE IEEE.2023
 - **MC-ELMM: Multi-Chip Endurance-Limited Memory Management**
Bartolo, A. M., Aly, M., Michelogiannakis, G., Mitra, S., Assoc Computing Machinery ASSOC COMPUTING MACHINERY.2023
 - **Thermal Scaffolding for Ultra-Dense 3D Integrated Circuits**
Rich, D., Kasperovich, A., Malakoutian, M., Radway, R. M., Hagiwara, S., Yoshikawa, T., Chowdhury, S., Mitra, S., IEEE IEEE.2023
 - **EMBER: A 100 MHz, 0.86 mm², Multiple-Bits-per-Cell RRAM Macro in 40 nm CMOS with Compact Peripherals and 1.0 pJ/bit Read Circuitry**
Upton, L. R., Levy, A., Scott, M. D., Rich, D., Khwa, W., Chih, Y., Chang, M., Mitra, S., Raina, P., Murmann, B., IEEE IEEE.2023: 469-472
 - **G-QED: Generalized QED Pre-silicon Verification beyond Non-Interfering Hardware Accelerators**
Chattopadhyay, S., Devarajegowda, K., Zhao, B., Lonsing, F., D'Agostino, B. A., Vavelidou, I., Bhatt, V. D., Prebeck, S., Ecker, W., Trippel, C., Barrett, C., Mitra, S., IEEE IEEE.2023
 - **Efficient Modeling and Calibration of Multi-Electrode Stimuli for Epiretinal Implants**
Vasireddy, P. K., Gogliettino, A. R., Brown, J. B., Vilku, R. S., Madugula, S. S., Phillips, A. J., Mitra, S., Hottowy, P., Sher, A., Litke, A., Shah, N. P., Chichilnisky, E. J., IEEE IEEE.2023
 - **Partitioned Temporal Dithering for Efficient Epiretinal Electrical Stimulation**
Lotlikar, A., Shah, N. P., Gogliettino, A. R., Vilku, R., Madugula, S., Grosberg, L., Hottowy, P., Sher, A., Litke, A., Chichilnisky, E. J., Mitra, S., IEEE IEEE.2023
 - **Testbench on a Chip: A Yield Test Vehicle for Resistive Memory Devices**
Upton, L. R., Lallement, G., Scott, M. D., Taylor, J., Radway, R. M., Rich, D., Nelson, M., Mitra, S., Murmann, B., IEEE IEEE.2023: 576-582
 - **Ultra-Dense 3D Physical Design Unlocks New Architectural Design Points with Large Benefits**

Srimani, T., Radway, R. M., Kim, J., Prabhu, K., Rich, D., Gilardi, C., Raina, P., Shulaker, M., Lim, S., Mitra, S.
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- **Three-Dimensional Stacked Neural Network Accelerator Architectures for AR/VR Applications** *IEEE MICRO*
Yang, L., Radway, R., Chen, Y., Wu, T., Liu, H., Ansari, E., Chandra, V., Mitra, S., Beigne, E.
2022; 42 (6): 116-124
- **Extended Scale Length Theory for Low-Dimensional Field-Effect Transistors** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Gilardi, C., Bennett, R. K. A., Yoon, Y., Pop, E., Wong, H., Mitra, S.
2022
- **Bandgap Extraction at 10 K to Enable Leakage Control in Carbon Nanotube MOSFETs** *IEEE ELECTRON DEVICE LETTERS*
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2022; 43 (3): 490-493
- **CHIMERA: A 0.92-TOPS, 2.2-TOPS/W Edge AI Accelerator With 2-MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
Prabhu, K., Gural, A., Khan, Z. F., Radway, R. M., Giordano, M., Koul, K., Doshi, R., Kustin, J. W., Liu, T., Lopes, G. B., Turbiner, V., Khwa, W., Chih, et al
2022
- **PEPR: Pseudo-Exhaustive Physically-Aware Region Testing**
Li, W., Nigh, C., Duvalsaint, D., Mitra, S., Blanton, R. D., IEEE Comp Soc
IEEE COMPUTER SOC.2022: 314-323
- **RADAR: A Fast and Energy-Efficient Programming Technique for Multiple Bits-Per-Cell RRAM Arrays** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Le, B. Q., Levy, A., Wu, T. F., Radway, R. M., Hsieh, E., Zheng, X., Nelson, M., Raina, P., Wong, H., Wong, S., Mitra, S.
2021; 68 (9): 4397-4403
- **Split-Chip Design to Prevent IP Reverse Engineering** *IEEE DESIGN & TEST*
Pagliarini, S., Sweeney, J., Mai, K., Blanton, S., Pileggi, L., Mitra, S.
2021; 38 (4): 109-118
- **Illusion of large on-chip memory by networked computing chips for neural network inference** *NATURE ELECTRONICS*
Radway, R. M., Bartolo, A., Jolly, P. C., Khan, Z. F., Le, B. Q., Tandon, P., Wu, T. F., Xin, Y., Vianello, E., Vivet, P., Nowak, E., Wong, H., Aly, et al
2021
- **Automatic Identification of Axon Bundle Activation for Epiretinal Prosthesis** *IEEE TRANSACTIONS ON NEURAL SYSTEMS AND REHABILITATION ENGINEERING*
Tandon, P., Bhaskhar, N., Shah, N., Madugula, S., Grosberg, L., Fan, V. H., Hottoway, P., Sher, A., Litke, A. M., Chichilnisky, E. J., Mitra, S.
2021; 29: 2496-2502
- **Spatially Patterned Bi-electrode Epiretinal Stimulation for Axon Avoidance at Cellular Resolution.** *Journal of neural engineering*
Vilkhu, R. S., Madugula, S. S., Grosberg, L. E., Gogliettino, A. R., Hottoway, P., Dabrowski, W., Sher, A., Litke, A. M., Mitra, S., Chichilnisky, E. J.
2021
- **Molybdenum oxide on carbon nanotube: Doping stability and correlation with work function** *JOURNAL OF APPLIED PHYSICS*
Park, R., Kim, H., Pitner, G., Neumann, C., Mitra, S., Wong, H.
2020; 128 (4)
- **A Density Metric for Semiconductor Technology** *PROCEEDINGS OF THE IEEE*
Wong, H., Akarvardar, K., Antoniadis, D., Bokor, J., Hu, C., King-Liu, T., Mitra, S., Plummer, J. D., Salahuddin, S.
2020; 108 (4): 478-82
- **Gap-free Processor Verification by S(2)QED and Property Generation**
Devarajegowda, K., Fadiheh, M., Singh, E., Barrett, C., Mitra, S., Ecker, W., Stoffel, D., Kunz, W.
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IEEE.2020: 526-31

- **Sensory Particles with Optical Telemetry**
Ganesan, K., Flores, T. A., Le, B. Q., Muratore, D. G., Patel, N., Mitra, S., Murmann, B., Palanker, D., IEEE
IEEE.2020
- **Cross-layer resilience** *CROSS-LAYER RELIABILITY OF COMPUTING SYSTEMS*
Cheng, E., Mitra, S.
edited by DiNatale, G., Gizopoulos, D., DiCarlo, S., Bosio, A., Canal, R.
2020; 57: 113-153
- **DECOY: Deflection-Driven HLS-Based Computation Partitioning for Obfuscating Intellectual Property**
Chen, J., Zaman, M., Makris, Y., Blanton, R., Mitra, S., Schafer, B., IEEE
IEEE.2020
- **A Formal Approach for Detecting Vulnerabilities to Transient Execution Attacks in Out-of-Order Processors**
Fadiheh, M., Mueller, J., Brinkmann, R., Mitra, S., Stoffel, D., Kunz, W., IEEE
IEEE.2020
- **A-QED Verification of Hardware Accelerators**
Singh, E., Lonsing, F., Chattopadhyay, S., Strange, M., Wei, P., Zhang, X., Zhou, Y., Chen, D., Cong, J., Raina, P., Zhang, Z., Barrett, C., Mitra, et al
IEEE.2020
- **A Data-Compressive Wired-OR Readout for Massively Parallel Neural Recording**
Muratore, D., Tandon, P., Wootters, M., Chichilnisky, E. J., Mitra, S., Murmann, B.
IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2019: 1128–40
- **Monolithic 3-D Integration** *IEEE MICRO*
Bishop, M. D., Wong, H., Mitra, S., Shulaker, M. M.
2019; 39 (6): 16–27
- **Hybrid Quick Error Detection: Validation and Debug of SoCs Through High-Level Synthesis** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
Campbell, K., Lin, D., He, L., Yang, L., Gurumani, S. T., Rupnow, K., Mitra, S., Chen, D.
2019; 38 (7): 1345–58
- **Resistive RAM Endurance: Array-Level Characterization and Correction Techniques Targeting Deep Learning Applications** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Grossi, A., Vianello, E., Sabry, M. M., Barlas, M., Grenouillet, L., Coignus, J., Beigne, E., Wu, T., Le, B. Q., Wootters, M. K., Zambelli, C., Nowak, E., Mitra, et al
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- **Low-Temperature Side Contact to Carbon Nanotube Transistors: Resistance Distributions Down to 10 nm Contact Length** *NANO LETTERS*
Pitner, G., Hills, G., Llinas, J., Persson, K., Park, R., Bokor, J., Mitra, S., Wong, H.
2019; 19 (2): 1083–89
- **Optimization of Electrical Stimulation for a High-Fidelity Artificial Retina**
Shah, N. P., Madugula, S., Grosberg, L., Mena, G., Tandon, P., Hottowy, P., Sher, A., Litke, A., Mitra, S., Chichilnisky, E. J., IEEE
IEEE.2019: 714–18
- **Unlocking the Power of Formal Hardware Verification with CoSA and Symbolic QED**
Lonsing, F., Ganesan, K., Mann, M., Nuthakki, S., Singh, E., Srouji, M., Yang, Y., Mitra, S., Barrett, C., IEEE
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- **Cross-Layer Resilience: Challenges, Insights, and the Road Ahead**
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- **A Data-Compressive Wired-OR Readout for Massively Parallel Neural Recording**
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- **Resistive RAM With Multiple Bits Per Cell: Array-Level Demonstration of 3 Bits Per Cell** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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- **A 43pJ/Cycle Non-Volatile Microcontroller with 4.7 μ s Shutdown/Wake-up Integrating 2.3-bit/Cell Resistive RAM and Resilience Techniques**
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- **The N3XT Approach to Energy-Efficient Abundant-Data Computing** *PROCEEDINGS OF THE IEEE*
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- **Processor Hardware Security Vulnerabilities and their Detection by Unique Program Execution Checking**
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- **Symbolic QED Pre-silicon Verification for Automotive Microcontroller Cores: Industrial Case Study**
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- **Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI** *IEEE TRANSACTIONS ON NANOTECHNOLOGY*
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- **Hyperdimensional Computing Exploiting Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D Integration** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
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2018; 53 (11): 3183–96
- **ETISS-ML: A Multi-Level Instruction Set Simulator with RTL-level Fault Injection Support for the Evaluation of Cross-Layer Resiliency Techniques**
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