Stanford

William Dally

Professor (Research) of Computer Science and of Electrical Engineering

CONTACT INFORMATION

- **Administrator**

  Mary Jane Swension - Executive Assistant

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  Tel (650) 723-0748

Bio

BIO

Dally develops efficient hardware for demanding information processing problems and sustainable energy systems. His current projects include domain-specific accelerators for deep learning, bioinformatics, and SAT solving; redesigning memory systems for the data center; developing efficient methods for video perception; and developing efficient sustainable energy systems. His research involves demonstrating novel concepts with working systems. Previous systems include the MARS Hardware Accelerator, the Torus Routing Chip, the J-Machine, M-Machine, the Reliable Router, the Imagine signal and image processor, the Merrimac supercomputer, and the ELM embedded processor. His work on stream processing led to GPU computing. His group has pioneered techniques including fast capability-based addressing, processor coupling, virtual channel flow control, wormhole routing, link-level retry, message-driven processing, deadlock-free routing, pruning neural networks, and quantizing neural networks.

ACADEMIC APPOINTMENTS

- Professor-Research, Computer Science
- Professor-Research, Electrical Engineering
- Member, Bio-X

BOARDS, ADVISORY COMMITTEES, PROFESSIONAL ORGANIZATIONS

- Member, American Academy of Arts and Sciences (2009 - present)
- Member, National Academy of Engineering (2010 - present)

PROFESSIONAL EDUCATION

- PhD, Caltech (1986)

LINKS

- http://cva.stanford.edu/billd_webpage_new.html: http://cva.stanford.edu/billd_webpage_new.html

Teaching

COURSES

2017-18

- Green Electronics: EE 155, EE 255 (Aut)

2016-17

- Green Electronics: EE 155, EE 255 (Aut)

STANFORD ADVISEES

Doctoral Dissertation Reader (AC)

Sneha Goenka

Doctoral Dissertation Advisor (AC)

Francis Chen, Huizi Mao, Chenzhuo Zhu

Doctoral (Program)

Huizi Mao, Chenzhuo Zhu

Publications

PUBLICATIONS

- **INVITED: Bandwidth-Efficient Deep Learning**
  Han, S., Dally, W. J., IEEE
  IEEE.2018
- **CG-OoO: Energy-Efficient Coarse-Grain Out-of-Order Execution Near In-Order Energy with Near Out-of-Order Performance** *ACM TRANSACTIONS ON ARCHITECTURE AND CODE OPTIMIZATION*
  Mohammadi, M., Aamodt, T. M., Dally, W. J.
  2017; 14 (4)
- **Conference Author/Panelist Index**
  Dally, W. J., Aoki, N., Bai, X., Banerjee, K., Benini, L., Bergamaschi, R.
- **Logic Simulation Algorithms for Pipelined Hardware Architectures** *Hardware Accelerators for Electrical CAD*
  Agrawal, P., Dally, W. J., Tutundjian, R.
  edited by Ambler, T., Agrawal, P.
  1988.
- **The Recon#gurable Arithmetic Processor**
  Fiske, S., Dally, W. J.
- **IEEE Fellows Lead the Engineering Profession**
  Dally, W. J., Agha, G. A., Babic, H. I., Basu, S., Beausoleil, W. F., Bertino, E.
- **Message-Driven Processor Architecture: Verson 11**
  Dally, W. J., Chien, A., Fiske, S., Horwat, W., Keen, J., Nuth, P.
- **ISSCC 2004/SESSION 7/TD: SCALING TRENDS/7.1**
  Horowitz, M., Dally, W.
- **CIMI FÍITIIt**
  Dally, W. J., Balfour, J., Black-Shaffer, D., Chen, J., Harting, R. C., Parikb, V.

- **AI Memo No. 1272 April 26, 1994**
  Spertus, E., Dally, W. J.
- **6 Guest Editors' Introduction: Top Picks from the 2008 Computer Architecture Conferences Joel Emer and Dean Tullsen 10 Larrabee: A Many-Core x86 Architecture**
  Dally, W. J., Seiler, L., Carmean, D., Sprangle, E., Forsyth, T., Abrash, M.
- **2010 Reviewers List**
  Dally, W. J., Acacio, M. E., Agrawal, N., Altman, E., Alur, R., Baas, B.
- **Stanford University Concurrent VLSI Architecture Memo 124 Elastic Buffer Networks-on-Chip**
  Michelogiannakis, G., Balfour, J., Dally, W. J.
- **Spills, Fills, and Kills**
  Erez, M., Towles, B. P., Dally, W. J.
- **ARVLSI'97 Committees**
  Dally, W. J., Brown, R. B., Ishii, A. T., Papaefthymiou, M. C., Mudge, T. N., June, C. S.
- **5 Guest Editors' Introduction: Hot Chips 21 Krste Asanovic and Ralph Wittig 7 Power7: IBM's Next-Generation Server Processor**
  Dally, W. J., Kalla, R., Sinharoy, B., Starke, W. J., Floyd, M., Conway, P.
- **31st Annual International Symposium on Computer Architecture ISCA 2004**
  Dally, W. J., Agerwala, T., Taylor, M., Lee, W., Miller, J., Wentzlaff, D.
- **SSCS Members Honored as 2002 IEEE Fellows**
  Banu, M., Burghartz, J. N., Dally, W. J., Dean, M. E., Gielen, G. G., Griffin, E. L.
- **ISSCC 2007/SESSION 24/MULTI-GB/s TRANSCEIVERS/24.3**
  Palmer, R., Poulton, J., Dally, W. J., Eyles, J., Fuller, A. M., Greer, T.
- **Globally Adaptive Load-Balanced Routing on k-ary n-cubes**
  Singh, A., Dally, W. J., Towles, B., Gupta, A. K.
- **1987 INDEX, VOLUME 4**
  Dally, W. J., Agrawal, P.
- **Program Chair's Message**
  Dally, W. J.
- **IEEE MICRO 1998 ANNUAL INDEX, VOL. 18** *Burns*
  Dally, W. J., Adams, J., Alt, P. M., Arai, T., Arakawa, F., Avresky, D. R.
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- **FPGAS VERSUS GPUS IN DATACENTERS** *IEEE MICRO*
  Falsafi, B., Dally, B., Singh, D., Chiou, D., Yi, J. J., Sendag, R.
  2017; 37 (1): 60-72
- **Exploring the Granularity of Sparsity in Convolutional Neural Networks**
  Mao, H., Han, S., Pool, J., Li, W., Liu, X., Wang, Y., Dally, W. J., IEEE
  IEEE.2017: 1927–34
- **SCNN: An Accelerator for Compressed-sparse Convolutional Neural Networks**
  Parashar, A., Rhu, M., Mukkara, A., Puglielli, A., Venkatesan, R., Khailany, B., Emer, J., Keckler, S. W., Dally, W. J., Assoc Comp Machinery
  ASSOC COMPUTING MACHINERY.2017: 27–40
- **Reuse Distance-Based Probabilistic Cache Replacement** *ACM TRANSACTIONS ON ARCHITECTURE AND CODE OPTIMIZATION*
  Das, S., Aamodt, T. M., Dally, W. J.
  2016; 12 (4)

- **On-Chip Active Messages for Speed, Scalability, and Efficiency** *IEEE TRANSACTIONS ON PARALLEL AND DISTRIBUTED SYSTEMS*
  Harting, R. C., Dally, W. J.
  2015; 26 (2): 507-515
- **On-Demand Dynamic Branch Prediction** *IEEE COMPUTER ARCHITECTURE LETTERS*
  Mohammadi, M., Han, S., Aamodt, T. M., Dally, W. J.
  2015; 14 (1): 50-53
- **A 0.54 pJ/b 20 Gb/s Ground-Referenced Single-Ended Short-Reach Serial Link in 28 nm CMOS for Advanced Packaging Applications** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Poulton, J. W., Dally, W. J., Chen, X., Eyles, J. G., Greer, T. H., Tell, S. G., Wilson, J. M., Gray, C. T.
  2013; 48 (12): 3206-3218
- **Elastic Buffer Flow Control for On-Chip Networks** *IEEE TRANSACTIONS ON COMPUTERS*
  Michelogiannakis, G., Dally, W. J.
  2013; 62 (2): 295-309
- **21st century digital design tools**
  Dally, W. J., Malachowsky, C., Keckler, S. W.
  2013
- **A 0.54 pJ/b 20Gb/s ground-referenced single-ended short-haul serial link in 28nm CMOS for advanced packaging applications** *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*
  Poulton, J. W., Dally, W. J., Chen, X., Eyles, J. G., Greer, T. H., Tell, S. G.
  2013
- **A detailed and flexible cycle-accurate network-on-chip simulator** *Performance Analysis of Systems and Software (ISPASS)*
  Jiang, N., Becker, D. U., Michelogiannakis, G., Balfour, J., Towles, B., Shaw, D. E.
  2013
- **A 0.54 pJ/b 20 Gb/s Ground-Referenced Single-Ended Short-Reach Serial Link in 28 nm CMOS for Advanced Packaging Applications** *IEEE*
  Poulton, J. W., Dally, W. J., Chen, X., Eyles, J. G., Greer, T. H., Tell, S. G.
  2013
- **Composition and reuse with compiled domain-specific languages**
  Dally, W. J., Sujeeth, A. K., Rompf, T., Brown, K. J., Lee, H., Chafi, H.
  2013
- **Optimizing data structures in high-level programs: new directions for extensible compilers based on staging**
  Rompf, T., Sujeeth, A. K., Amin, N., Brown, K. J., Jovanovic, V., Lee, H.
  2013
- **Channel reservation protocol for over-subscribed channels and destinations**
  Michelogiannakis, G., Jiang, N., Becker, D., Dally, W. J.
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- **A Hierarchical Thread Scheduler and Register File for Energy-Efficient Throughput Processors** *ACM TRANSACTIONS ON COMPUTER SYSTEMS*
  Gebhart, M., Johnson, D. R., Tarjan, D., Keckler, S. W., Dally, W. J., Lindholm, E., Skadron, K.
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- **Green-Marl: A DSL for Easy and Efficient Graph Analysis** *ACM SIGPLAN NOTICES*
  Hong, S., Chafi, H., Sedlar, E., Olukotun, K.
  2012; 47 (4): 349-362
- **Network Congestion Avoidance Through Speculative Reservation** *18th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*
  Jiang, N., Becker, D. U., Michelogiannakis, G., Dally, W. J.
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- **A case of system-level hardware/software co-design and co-verification of a commodity multi-processor system with custom hardware**
  Dally, W. J., Hong, S., Oguntebi, T., Casper, J., Bronson, N., Kozyrakis, C.

2012

- **Digital Design: A Systems Approach**
  Dally, W. J., Harting, R. C.
  Cambridge University Press.2012
- **Unifying primary cache, scratch, and register file memories in a throughput processor**
  Gebhart, M., Keckler, S. W., Khailany, B., Krashinsky, R., Dally, W. J.
  2012
- **Article 8-A Hierarchical Thread Scheduler and Register File for Energy-Efficient Throughput Processors** *ACM Transactions on Computer Systems-TOCS*
  Gebhart, M., Johnson, D. R., Tarjan, D., Keckler, S. W., Dally, W. J., Lindholm, E.
  2012; 2 (30): 38
- **It's about the Power: An Architect's View of Interconnect** *IEEE International Interconnect Technology Conference (IITC)*
  Dally, B.
  IEEE.2012
- **Adaptive Backpressure: Efficient Buffer Management for On-Chip Networks** *30th IEEE International Conference on Computer Design (ICCD)*
  Becker, D. U., Jiang, N., Michelogiannakis, G., Dally, W. J.
  IEEE.2012: 419–426
- **Packet Chaining: Efficient Single-Cycle Allocation for On-Chip Networks** *IEEE COMPUTER ARCHITECTURE LETTERS*
  Michelogiannakis, G., Jiang, N., Becker, D. U., Dally, W. J.
  2011; 10 (2): 33-36
- **Evaluating Elastic Buffer and Wormhole Flow Control** *IEEE TRANSACTIONS ON COMPUTERS*
  Michelogiannakis, G., Becker, D. U., Dally, W. J.
  2011; 60 (6): 896-903
- **4 Guest Editor’s Introduction: CPUs, GPUs, and Hybrid Computing David Brooks 7 GPUs and the Future of Parallel Computing**
  Keckler, S. W., Dally, W. J., Khailany, B., Garland, M., Glasco, D., Rohr, D.
  2011
- **Guaranteeing forward progress of unified register allocation and instruction scheduling** *Technical Report Concurrent VLSI Architecture Group Memo 127, Stanford*
  Park, J., Dally, W. J.
  2011
- **Gpus and the future of parallel computing** *Micro, IEEE*
  Keckler, S. W., Dally, W. J., Khailany, B., Garland, M., Glasco, D.
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- **Energy-efficient mechanisms for managing thread context in throughput processors** *ACM SIGARCH Computer Architecture News*
  Gebhart, M., Johnson, D. R., Tarjan, D., Keckler, S. W., Dally, W. J., Lindholm, E.
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- **2011 Index IEEE Computer Architecture Letters Vol. 10** *Computer Architecture Letters*
  Becker, D., Choi, I., Cooper-Balis, E., Dally, W. J., Devadas, S., Duato, J.
  2011; 53: 56
- **Circuit challenges for future computing systems**
  Dally, W. J.
  2011
- **Liszt: a domain specific language for building portable mesh-based PDE solvers**
  DeVito, Z., Joubert, N., Palacios, F., Oakley, S., Medina, M., Barrientos, M.
  2011
- **A compile-time managed multi-level register file hierarchy**
  Gebhart, M., Keckler, S. W., Dally, W. J.

2011

- **Efficient Topologies for Large-scale Cluster Networks** *Conference on Optical Fiber Communication (OFC)/Collocated National Fiber Optic Engineers (NFOEC)*
  Kim, J., Dally, W. J., Abts, D.
  IEEE.2010
- **Throughput computing**
  Dally, W. J.
  2010
- **Evaluating bufferless flow control for on-chip networks**
  Michelogiannakis, G., Sanchez, D., Dally, W. J., Kozyrakis, C.
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- **The even/odd synchronizer: A fast, all-digital, periodic synchronizer** *Asynchronous Circuits and Systems (ASYNC), 2010 IEEE Symposium on*
  Dally, W. J., Tell, S. G.
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- **Moving the needle, computer architecture research in academe and industry** *ACM SIGARCH Computer Architecture News*
  Dally, W. J.
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- **Booksim 2.0 User's Guide** *Standford University*
  Jiang, N., Michelogiannakis, G., Becker, D., Towles, B., Dally, W. J.
  2010
- **The end of denial architecture and the rise of throughput computing**
  Dally, W. J.
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- **The GPU Computing Era (HTML)**
  Nickolls, J., Dally, W. J.
  2010
- **Fine-grain dynamic instruction placement for L0 scratch-pad memory**
  Park, J., Balfour, J., Dally, W. J.
  2010
- **Block-Parallel Programming for Real-time Embedded Applications**
  WJ
  2010
- **Apparatus and method for packet scheduling** *US Patent*
  Dally, W. J., Carvey, P. P., Beliveau, P. A., Mann, W. F., Dennison, L. R.
  2010; 760 (7): 747
- **2010 IEEE Symposium on Asynchronous Circuits and Systems**
  Dally, W. J., Tell, S. G.
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- **The GPU computing era** *Micro, IEEE*
  Nickolls, J., Dally, W. J.
  2010; 2 (30): 56-69
- **The end of denial architecture and the rise of throughput computing** *Keynote speech at Desgin Automation Conference*
  Dally, W. J.
  2010
- **Buffer-space Efficient and Deadlock-free Scheduling of Stream Applications on Multi-core Architectures** *22nd ACM Symposium on Parallelism in Algorithms and Architectures*

Park, J., Dally, W. J.
ASSOC COMPUTING MACHINERY.2010: 1–10

- **Operand Registers and Explicit Operand Forwarding** *IEEE COMPUTER ARCHITECTURE LETTERS*
  Balfour, J., Harting, R. C., Dally, W. J.
  2009; 8 (2): 60-63
- **COST-EFFICIENT DRAGONFLY TOPOLOGY FOR LARGE-SCALE SYSTEMS** *IEEE MICRO*
  Kim, J., Dally, W., Scott, S., Abts, D.
  2009; 29 (1): 33-40
- **Indirect adaptive routing on large scale interconnection networks** *ACM SIGARCH Computer Architecture News*
  Jiang, N., Kim, J., Dally, W. J.
  2009; 3 (37): 220-231
- **Router designs for elastic buffer on-chip networks**
  Michelogiannakis, G., Dally, W. J.
  2009
- **Embracing heterogeneity–parallel programming for changing hardware**
  Linderman, M. D., Balfour, J., Meng, T. H., Dally, W. J.
  2009
- **Power efficient supercomputing** *Accelerator-based Computing and Manycore Workshop (presentation)*
  Dally, W. J.
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- **Elastic-buffer flow control for on-chip networks** *High Performance Computer Architecture*
  Michelogiannakis, G., Balfour, J., Dally, W. J.
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- **Allocator implementations for network-on-chip routers**
  Becker, D. U., Dally, J. J.
  2009
- **Maximizing the Filter Rate of L0 Compiler-Managed Instruction Stores by Pinning** *Technical Report 126, Concurrent VLSI Architecture Group, Stanford University*
  Park, J., Balfour, J., Dally, W. J.
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- **Stream Processors** *Multicore Processors and Systems*
  Erez, M., Dally, W. J.
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- **Load-balanced routing** *US Patent*
  Singh, A., Dally, W. J.
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- **Exascale software study: Software challenges in extreme scale systems** *DARPA IPTO, Air Force Research Labs*
  Amarasinghe, S., Campbell, D., Carlson, W., Chien, A., Dally, W., Elnohazy, E.
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- **Elastic-Buffer Flow Control for On-Chip Networks** *15th International Symposium on High-Performance Computer Architecture*
  Michelogiannakis, G., Balfour, J., Dally, W. J.
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- **Opportunities Beyond Single-Core Microprocessors** *15th International Symposium on High-Performance Computer Architecture*
  Hill, M. D., Adve, S. V., Bader, D. A., Dally, W., Harrod, W., Sarkar, V.
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- **Efficient embedded computing** *COMPUTER*
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  Das, A., Dally, W. J.
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- **A tuning framework for software-managed memory hierarchies**
  Ren, M., Park, J. Y., Houston, M., Aiken, A., Dally, W. J.
  2008
- **An energy-efficient processor architecture for embedded systems** *Computer Architecture Letters*
  Balfour, J., Dally, W. J., Black-Schaffer, D., Parikh, V., Park, J. S.
  2008; 1 (7): 29-32
- **Exascale computing study: Technology challenges in achieving exascale systems**
  Kogge, P., Bergman, K., Borkar, S., Campbell, D., Carson, W., Dally, W.
  2008
- **A programmable 512 GOPS stream processor for signal, image, and video processing** *Solid-State Circuits, IEEE Journal*
  Khailany, B. K., Williams, T., Lin, J., Long, E. P., Rygh, M., Tovey, D. F., Dally, B.
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- **Structured Application-Specific Integrated Circuit (ASIC) Study** *STANFORD UNIV CA COMPUTER SYSTEMS LAB*
  Dally, W., Balfour, J., Black-Schaffer, D., Hartke, P.
  2008
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  2008
- **Hierarchical instruction register organization** *Computer Architecture Letters*
  Black-Schaffer, D., Balfour, J., Dally, W., Parikh, V., Park, J. S.
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- **A Portable Runtime Interface For Multi-Level Memory Hierarchies** *ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP 08)*
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- **Technology-driven, highly-scalable dragonfly topology** *35th Annual International Symposium on Computer Architecture*
  Kim, J., Dally, W. J., Scott, S., Abts, D.
  IEEE COMPUTER SOC.2008: 77–88
- **A 14-mW 6.25-Gb/s transceiver in 90-nm CMOS** *IEEE International Solid-State Circuits Conference (ISSCC)*
  Poulton, J., Palmer, R., Fuller, A. M., Greer, T., Eyles, J., Dally, W. J., Horowitz, M.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2007: 2745–57
- **Research challenges for on-chip interconnection networks** *IEEE MICRO*
  Owens, J. D., Dally, W. J., Ho, R., Jayasimha, D. N., Keckler, S. W., Peh, L.
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- **Register pointer architecture for efficient embedded processors** *Design, Automation and Test in Europe Conference and Exhibition (DATE 07)*
  Park, J., Park, S., Balfour, J. D., Black-Schaffer, D., Kozyrakis, C., Dally, W. J.
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- **Research Challenges for On-Chip Interconnection Networks (HTML)**
  Owens, J. D., Dally, W. J., Ho, R., Jayasimha, D. N., Keckler, S. W., Peh, L. S.
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- **Executing irregular scientific applications on stream architectures**
  Erez, M., Ahn, J. H., Gummaraju, J., Rosenblum, M., Dally, W. J.
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- **A 14mW 6.25 Gb/s transceiver in 90nm CMOS for serial chip-to-chip communications**
  Palmer, R., Poulton, J., Dally, W. J., Eyles, J., Fuller, A. M., Greer, T.
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- **Architectural support for the stream execution model on general-purpose processors**
  Gummaraju, J., Erez, M., Coburn, J., Rosenblum, M., Dally, W. J.
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- **Stream Scheduling: A Framework to Manage Bulk Operations in a Memory Hierarchy** *Parallel Architecture and Compilation Techniques*
  Das, A., Dally, W. J.
  2007
- **Interconnect-Centric Computing.** *HPCA*
  Dally, W. J., Keynote, H.
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- **Tradeoff between data-, instruction-, and thread-level parallelism in stream processors**
  Ahn, J., Erez, M., Dally, W. J.
  2007
- **Flattened butterfly: a cost-efficient topology for high-radix networks** *ACM SIGARCH Computer Architecture News*
  Kim, J., Dally, W. J., Abts, D.
  2007; 2 (35): 126-137
- **Computer architecture in the many-core era** *24th International Conference on Computer Design*
  Dally, B.
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- **Compilation for Explicitly Managed Memory Hierarchies** *ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*
  Knight, T. J., Park, J. Y., Ren, M., Houston, M., Erez, M., Fatahalian, K., Aiken, A., Dally, W. J., Hanrahan, P.
  ASSOC COMPUTING MACHINERY.2007: 226–236
- **Flattened Butterfly : A Cost-Efficient Topology for High-Radix Networks** *34th Annual International Symposium on Computer Architecture*
  Kim, J., Dally, W. J., Abts, D.
  ASSOC COMPUTING MACHINERY.2007: 126–137
- **Flattened butterfly topology for on-chip networks** *40th Annual IEEE/AMC International Symposium on Microarchitecture*
  Kim, J., Balfour, J., Dally, W. J.
  IEEE COMPUTER SOC.2007: 172–182
- **The BlackWidow high-radix Clos network** *33rd International Symposium on Computer Architecture*
  Scott, S., Abts, D., Kim, J., Dally, W. J.
  IEEE COMPUTER SOC.2006: 16–27
- **Pulsenet - A parallel flash sampler and digital processor IC for optical SETI** *PROCEEDINGS OF THE IEEE 2006 CUSTOM INTEGRATED CIRCUITS CONFERENCE*
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  2006: 261-264
- **Sequoia: programming the memory hierarchy**
  Fatahalian, K., Horn, D., Knight, T., Leem, L., Houston, M., Park, J., Dally, B.
  2006

- **Multi-Core for HPC: Breakthrough or Breakdown?**
  Sterling, T., Kogge, P., Dally, W., Scott, S., Gropp, W., Keyes, D.
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- **Topology optimization of interconnection networks** *Computer Architecture Letters*
  Gupta, A. K., Dally, W. J.
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  Waters, G. M., Dennison, L. R., Carvey, P. P., Dally, W. J., Mann, W. F.
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- **DRAFT Final Report: Workshop on On-and Off-Chip Networks for Multi-Core Systems** *Capturado em: http://www. ece. ucdavis. edu/~ ocin06*
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  2006
- **Compiling for stream processing**
  Das, A., Dally, W. J., Mattson, P.
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- **Data parallel address architecture** *Computer Architecture Letters*
  Ahn, J. H., Dally, W. J.
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- **Adaptive routing in high-radix clos network**
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  Howard, A. W., Wei, G. Y., Dally, W. J., Horowitz, P.
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- **The design space of data-parallel memory systems**
  Ahn, J. H., Erez, M., Dally, W. J.
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- **Design tradeoffs for tiled CMP on-chip networks**
  Balfour, J., Dally, W., J.
  2006
- **Future directions for on-chip interconnection networks** *OCIN Workshop*
  Dally, W. J.
  2006
- **A 20-Gb/s 0.13-mu m CMOS serial link transmitter using an LC-PLL to directly drive the output multiplexer** *Symposium on VLSI Circuits*
  Chiang, P., Dally, W. J., Lee, M. J., Senthinathan, R., Oh, Y., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2005: 1004–11
- **Scatter-add in data parallel architectures** *11th International Symposium on High-Performance Computer Architecture*
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