Stanford

S Simon Wong

Professor of Electrical Engineering

CONTACT INFORMATION

- **Administrative Contact**

  Meihua Xu - Administrative Assistant

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Bio

BIO

Wong studies the fabrication and design of high-performance integrated circuits. His work focuses on understanding and overcoming the limitations of circuit performance imposed by device, interconnect and on-chip components.

ACADEMIC APPOINTMENTS

- Professor, Electrical Engineering
- Member, Bio-X
- Member, Wu Tsai Neurosciences Institute

HONORS AND AWARDS

- Fellow, IEEE

BOARDS, ADVISORY COMMITTEES, PROFESSIONAL ORGANIZATIONS

- Board Director, Pericom Semiconductor (2006 - 2015)

PROFESSIONAL EDUCATION

- PhD, UC Berkeley (1983)

Research & Scholarship

CURRENT RESEARCH AND SCHOLARLY INTERESTS

Current research focuses on

Resistive Random Access Memory (RRAM) and Integration with CMOS

Energy Efficient Approximate Computing for Machine Learning

Teaching

COURSES

2019-20

- Circuits I: EE 101A (Win)
- Circuits II: EE 101B (Spr)

2018-19

- Circuits II: EE 101B (Spr)
- Introductory Electronics: ENGR 40A (Win)
- Introductory Electronics Part II: ENGR 40B (Win)

2017-18

- Circuits II: EE 101B (Spr)
- Introductory Electronics: ENGR 40A (Win)
- Introductory Electronics Part II: ENGR 40B (Win)

2016-17

- Introductory Electronics: ENGR 40A (Win)
- Introductory Electronics Part II: ENGR 40B (Win)

STANFORD ADVISEES

Doctoral Dissertation Reader (AC)

George Alexopoulos, Cheng Chen, Zizhen Jiang, Siavash Kananian, Ella Thomson, Tony Wu, Xin Zheng

Doctoral Dissertation Advisor (AC)

Fei Huang, Andrew Ma

Master's Program Advisor

Ruoyan Chen, Melissa Horowitz, Andrew Misiolek

Publications

PUBLICATIONS

- **Next-Generation Ultrahigh-Density 3-D Vertical Resistive Switching Memory (VRSM)-Part I: Accurate and Computationally Efficient Modeling** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Qin, S., Jiang, Z., Li, H., Fujii, S., Lee, D., Wong, S., Wong, H.
  2019; 66 (12): 5139–46
- **Next-Generation Ultrahigh-Density 3-D Vertical Resistive Switching Memory (VRSM)-Part II: Design Guidelines for Device, Array, and Architecture** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Jiang, Z., Qin, S., Li, H., Fujii, S., Lee, D., Wong, S., Wong, H.
  2019; 66 (12): 5147–54
- **DATASET CULLING: TOWARDS EFFICIENT TRAINING OF DISTILLATION-BASED DOMAIN SPECIFIC MODELS**
  Yoshioka, K., Lee, E., Wong, S., Horowitz, M., IEEE
  IEEE.2019: 3237–41
- **Deep learning to predict survival prognosis for patients with non-small cell lung cancer using images and clinical data**
  Lee, E. H., Zhou, M., Gamboa, N., Brennan, K., Itakura, H., Nair, V., Napel, S., Wong, S., Gevaert, O.

AMER ASSOC CANCER RESEARCH.2018

- **Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM**
  Jiang, Z., Qin, S., Li, H., Fujii, S., Lee, D., Wong, S., Wong, H., IEEE
  IEEE.2018: 107–8

- **Fault-Tolerant FPGA with Column-Based Redundancy and Power Gating Using RRAM** *IEEE TRANSACTIONS ON COMPUTERS*
  Lee, K., Wong, S. S.
  2017; 66 (6): 946-956

- **Analysis and Design of a Passive Switched-Capacitor Matrix Multiplier for Approximate Computing** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Lee, E. H., Wong, S. S.
  2017; 52 (1): 261-271

- **LOGNET: ENERGY-EFFICIENT NEURAL NETWORKS USING LOGARITHMIC COMPUTATION**
  Lee, E. H., Miyashita, D., Chai, E., Murmann, B., Wong, S., IEEE
  IEEE.2017: 5900–5904

- **TPAD: Hardware Trojan Prevention and Detection for Trusted Integrated Circuits** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Wu, T. F., Ganesan, K., Hu, Y. A., Wong, H. P., Wong, S., Mitra, S.
  2016; 35 (4): 521-534

- **A 2.5GHz 7.7TOPS/W Switched-Capacitor Matrix Multiplier with Co-designed Local Memory in 40nm**
  Lee, E. H., Wong, S., IEEE
  IEEE.2016: 418–U587

- **Fault-tolerant FPGA with Column-based Redundancy and Power Gating Using RRAM**
  Lee, K., Wong, S., IEEE
  IEEE.2016: 409–14

- **A Deep Learning Framework to Predict Survival from Medical Images of Lung Cancer Patients** *Conference on Neural Information Processing Systems, Workshop on Machine Learning for Health*
  Lee, E., Zhou, M., Grove, O., Balagurunathan, Y., Echegaray, S., Gillies, R., Gamboa, N., Murmann, B., Napel, S., Wong, S., Gevaert, O.
  2016

- **Monolithic 3-D FPGAs** *PROCEEDINGS OF THE IEEE*
  Zhang, Z., Liauw, Y. Y., Chen, C., Wong, S. S.
  2015; 103 (7): 1197-1210

- **Compact One-Transistor-N-RRAM Array Architecture for Advanced CMOS Technology** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Yeh, C. S., Wong, S. S.
  2015; 50 (5): 1299-1309

- **FACTORIZATION FOR ANALOG-TO-DIGITAL MATRIX MULTIPLICATION**
  Lee, E. H., Udell, M., Wong, S., IEEE
  IEEE.2015: 1061–65

- **All-Metal-Nitride RRAM Devices** *IEEE ELECTRON DEVICE LETTERS*
  Zhang, Z., Gao, B., Fang, Z., Wang, X., Tang, Y., Sohn, J., Wong, H. P., Wong, S. S., Lo, G.
  2015; 36 (1): 29-31

- **The Role of Ti Capping Layer in HfOx-Based RRAM Devices** *IEEE ELECTRON DEVICE LETTERS*
  Fang, Z., Wang, X. P., Sohn, J., Weng, B. B., Zhang, Z. P., Chen, Z. X., Tang, Y. Z., Lo, G., Provine, J., Wong, S. S., Wong, H. P., Kwong, D.
  2014; 35 (9): 912-914

- **Current Conduction Mechanism of Nitrogen-Doped AlOx RRAM** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Kim, W., Park, S. I., Zhang, Z., Wong, S.
  2014; 61 (6): 2158-2163

- **Low-Temperature Monolithic Three-Layer 3-D Process for FPGA** *IEEE ELECTRON DEVICE LETTERS*

Zhang, Z., Chen, C., Crnogorac, F., Chen, S., Griffin, P. B., Pease, R. F., Plummer, J. D., Wong, S. S.
2013; 34 (8): 1044-1046

- **Nanometer-Scale HfOx RRAM** *IEEE ELECTRON DEVICE LETTERS*
  Zhang, Z., Wu, Y., Wong, H. P., Wong, S. S.
  2013; 34 (8): 1005-1007
- **Impact of III-V and Ge Devices on Circuit Performance** *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS*
  Park, J., Oh, S., Kim, S., Wong, H. P., Wong, S. S.
  2013; 21 (7): 1189-1200
- **Effect of Wordline/Bitline Scaling on the Performance, Energy Consumption, and Reliability of Cross-Point Memory Array** *ACM JOURNAL ON EMERGING TECHNOLOGIES IN COMPUTING SYSTEMS*
  Liang, J., Yeh, S., Wong, S. S., Wong, H. P.
  2013; 9 (1)
- **Trusted Integrated Chips Integrating Non-Volatile Memory with CMOS**
  Provine, J., Wong, H., Wong, S., Mitra, S.
  2013
- **First Demonstration of RRAM Patterned by Block Copolymer Self-Assembly** *IEEE International Electron Devices Meeting (IEDM)*
  Wu, Y., Yi, H., Zhang, Z., Jiang, Z., Sohn, J., Wong, S., Wong, H. P.
  IEEE.2013
- **Characterization of Geometric Leakage Current of GeO2 Isolation and Effect of Forming Gas Annealing in Germanium p-n Junctions** *IEEE ELECTRON DEVICE LETTERS*
  Jung, W., Park, J., Lin, J. J., Wong, S., Saraswat, K. C.
  2012; 33 (11): 1520-1522
- **A superheterodyne receiver front-end with on-chip automatically Q-tuned notch filters** *ANALOG INTEGRATED CIRCUITS AND SIGNAL PROCESSING*
  Chi, B., Wang, Z., Wong, S. S.
  2012; 71 (3): 453-463
- **Nonvolatile 3D-FPGA with Monolithically Stacked RRAM-Based Configuration Memory**
  Yang-Liauw, Y., Zhang, Z., Kim, W., El-Gamal, A., Wong, S.
  2012
- **Scaling Challenges for the Cross-point Resistive Memory Array to Sub-10nm Node - An Interconnect Perspective** *4th IEEE International Memory Workshop (IMW)*
  Liang, J., Yeh, S., Wong, S. S., Wong, H. P.
  IEEE.2012
- **Scaling Challenges for the Cross-point Resistive Memory Array to the Single-digit-nm Node – An Interconnect Perspective**
  Liang, S., Yip, S., Wong, H., S., Wong, P.
  2012
- **Array Architecture for a Nonvolatile 3-Dimensional Cross-Point Resistance-Change Memory** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Ou, E., Wong, S. S.
  2011; 46 (9): 2158-2170
- **A 65 nm CMOS fully-integrated dynamic reconfigurable differential power amplifier with high gain in both bands** *MICROELECTRONICS JOURNAL*
  Chi, B., Omid-Zohoor, K., Wang, Z., Wong, S. S.
  2011; 42 (6): 855-862
- **A 60GHz Digitally Controlled RF Beamforming Array in 65nm CMOS with Off-Chip Antennas**
  Lin, S., Ng, K., Wong, H., Luk, K., Wong, S., Poon, A.
  2011
- **Forming-Free Nitrogen-Doped AlOx RRAM with Sub-µA Programming Current**
  Kim, W., Park, S., I., Zhang, Z., Yang-Liauw, Y., Sekar, D., Wong, H., S. P.
  2011

- **3D Field Programmable Gate Array**
  Yang-Liauw, Y., Crnororac, F., Chen, E., Jung, W., Kim, W., Park, S., Wong, S. S.
  2011

- **Semiconductor crystal islands for three-dimensional integration** *54th International Conference on Electron, Ion and Photon Beam Technology and Nanofabrication*
  Crnogorac, F., Wong, S., Pease, R. F.
  A V S AMER INST PHYSICS.2010: C6P53-C6P58

- **Leakage Current Analysis of Lateral p+/n Ge Based Diode Activated at Low Temperature for Three-Dimensional Integrated Circuit (3D-ICs)**
  Jung, W., Park, J., Kuzum, D., Kim, W., Wong, S., Saraswat, K.
  2010

- **Leakage Current Analysis of Lateral p+/n Ge Based Diode Activated at Low Temperature for Three-Dimensional Integrated Circuit (3D-ICs)** *Symposium on Processing, Materials, and Integration of Damascene and 3D Interconnects held during the 218th Meeting of the Electrochemical-Society*
  Jung, W. S., Park, J., Kuzum, D., Kim, W., Wong, S., Saraswat, K. C.
  ELECTROCHEMICAL SOC INC.2010: 35–39

- **Optimization of Driver Preemphasis for On-Chip Interconnects** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS*
  Bai, Y., Wong, S. S.
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- **RESET Mechanism of TiOx Resistance-Change Memory Device** *IEEE ELECTRON DEVICE LETTERS*
  Wang, W., Fujita, S., Wong, S. S.
  2009; 30 (7): 733-735

- **Elimination of Forming Process for TiOx Nonvolatile Memory Devices** *IEEE ELECTRON DEVICE LETTERS*
  Wang, W., Fujita, S., Wong, S. S.
  2009; 30 (7): 763-765

- **Reduction of Inductive Crosstalk Using Quadrupole Inductors** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Poon, A., Chang, A., Samavati, H., Wong, S. S.
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- **Pi Coil: A New Element for Bandwidth Extension** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II-EXPRESS BRIEFS*
  Lin, S., Huang, D., Wong, S.
  2009; 56 (6): 454-458

- **A 60-GHz LOW-NOISE AMPLIFIER FOR 60-GHz DUAL-CONVERSION RECEIVER** *MICROWAVE AND OPTICAL TECHNOLOGY LETTERS*
  Lin, Y., Wong, S. S.
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- **The Prospect of 3D-IC** *IEEE Custom Integrated Circuits Conference*
  Wong, S. S., El Gamal, A.
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- **Low-Power 48-GHz CMOS VCO and 60-GHz CMOS LNA for 60-GHz Dual-Conversion Receiver** *2009 INTERNATIONAL SYMPOSIUM ON VLSI DESIGN, AUTOMATION AND TEST (VLSI-DAT), PROCEEDINGS OF TECHNICAL PROGRAM*
  Lin, Y., Chang, T., Chen, C., Chen, C., Yang, H., Wong, S. S.
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- **Low-Power 48-GHz CMOS VCO and 60-GHz CMOS LNA for 60-GHz Dual-Conversion Receiver**
  Lin, Y., Chang, T., Chen, C., Chen, C., Yang, H., Wong, S.
  2009

- **Performance Comparison between Capacitively Driven Low Swing and Conventional Interconnects for Cu and Carbon Nanotube Wire Technologies** *IEEE International Interconnect Technology Conference*
  Koo, K., Kapur, P., Park, J., Noh, H., Wong, S. S., Saraswat, K. C.
  IEEE.2009: 23–25

- **A High-Performance 3D-SRAM Architecture**
  Wong, S., Nho, H.
  2009
- **Numerical estimation of yield in sub-100-nm SRAM design using Monte Carlo simulation** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II-EXPRESS BRIEFS*
  Nho, H., Yoon, S., Wong, S. S., Jung, S.
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- **High-performance gate-all-around GeOI p-MOSFETs fabricated by rapid melt growth using plasma nitridation and ALD Al2O3 gate dielectric and self-aligned NiGe contacts** *IEEE ELECTRON DEVICE LETTERS*
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- **A High-speed, Low-power 3D-SRAM Architecture** *IEEE Custom Integrated Circuits Conference*
  Nho, H. H., Horowitz, M., Wong, S. S.
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- **A low-power V-band CMOS low-noise amplifier using current-sharing technique**
  Yang, H., Lin, Y., Chen, C., Wong, S. S., IEEE
  IEEE.2008: 964-+
- **A Low-Power V-Band CMOS Low Noise Amplifier using Current Sharing Technique**
  Yang, H., Lin, Y., Chen, C., Wong, S.
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- **Monolithic 3D Integrated Circuits**
  Wong, S., El-Gamal, A., Griffin, P., Nishi, Y., Pease, F., Plummer, J.
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- **An on-chip dipole antenna for millimeter-wave transmitters** *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*
  Park, P. H., Wong, S. S.
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- **Thickness and stoichiometry dependence of the thermal conductivity of GeSbTe films** *APPLIED PHYSICS LETTERS*
  Reifenberg, J. P., Panzer, M. A., Kim, S., Gibby, A. M., Zhang, Y., Wong, S., Wong, H. P., Pop, E., Goodson, K. E.
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- **Closed-form RC and RLC delay models considering input rise time** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS*
  Kim, S., Wong, S. S.
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- **Statistical simulation methodology for sub100 nm memory design** *ELECTRONICS LETTERS*
  Nho, H., Yoon, S., Wong, S., Jung, S.
  2007; 43 (16): 869-870
- **Performance benefits of monolithically stacked 3-D FPGA** *International Symposium on Field-Programmable Gate Arrays*
  Lin, M., El Gamal, A., Lu, Y., Wong, S.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2007: 216–29
- **Resistive switching mechanism in ZnxCd1-xS nonvolatile memory devices** *IEEE ELECTRON DEVICE LETTERS*
  Wang, Z., Griffin, P. B., McVittie, J., Wong, S., McIntyre, P. C., Nishi, Y.
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- **A superheterodyne receiver front-end with on-chip automatically Q-tuned notch filters** *2007 IEEE RADIO FREQUENCY INTEGRATED CIRCUITS (RFIC) SYMPOSIUM, DIGEST OF PAPERS*
  Chi, B., Wang, Z., Wong, S. S.
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- **A Fully Integrated RF Front-End with Independent RX/TX Matching and +20dbm Output Power for WLAN Applications**

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2007

- **Integrated transformer baluns for RF low noise and power amplifiers** *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*
  Gan, H., Wong, S. S.
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- **Nonvolatile SRAM Cell**
  Wang, W., Gibby, A., Wang, Z., Fujita, S., Griffin, P., Nishi, Y., Wong, S. S.
  2006
- **Performance Benefits of Monolithically Stacked 3D-FPGA**
  Lin, M., El Gamal, A., Lu, Y., Wong, S.
  2006
- **Multiphysics modeling and impact of thermal boundary resistance in phase change memory devices** *10th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*
  Reifenberg, J., Pop, E., Gibby, A., Wong, S., Goodson, K.
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  Gan, H., Wong, S. S.
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- **Analysis and synthesis of on-chip spiral inductors** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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  Yue, C. P., Wong, S. S.
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- **Modeling and optimization of substrate resistance for RF-CMOS** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Chang, R. T., Yang, M. T., Ho, P. P., Wang, Y. J., Chia, Y. T., Liew, B. K., Yue, C. P., Wong, S. S.
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- **A 10-GHz global clock distribution using coupled standing-wave oscillators** *IEEE International Solid-State Circuits Conference*
  O'Mahony, F., Yue, C. P., Horowitz, M. A., Wong, S. S.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2003: 1813–20
- **Near speed-of-light signaling over on-chip electrical interconnects** *Symposium on VLSI Circuits*
  Chang, R. T., Talwalkar, N., Yue, C. P., Wong, S. S.
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- **Near speed-of-light velocities for on-chip - transmission of electrical signals** *SOLID STATE TECHNOLOGY*
  Chang, R. T., Wong, S. S.
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- **Correlation of stress and texture evolution during self- and thermal annealing of electroplated Cu films** *JOURNAL OF APPLIED PHYSICS*
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- **On the accuracy of return path assumption for loop inductance extraction for 0.1 mu m technology and beyond** *4th IEEE International Symposium on Quality Electronic Design*
  Kim, S. Y., Massoud, Y., Wong, S. S.
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  Talwalkar, N., Yue, C., Wong, S.
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- **Mechanism for Early Failure in Cu Dual Damascene Structure**
  Kim, D., Wong, S.
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- **10GHz Clock Distribution Using Coupled Standing-Wave Oscillators**
  O'Mahony, F., Yue, C., Wong, S.
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- **Compact modeling of high frequency phenomena for on-chip spiral inductors** *Nanotechnology Conference and Trade Show (Nanotech 2003)*
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  O'Mahony, F., Yue, C. P., Horowitz, M. A., Wong, S. S.
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- **High-frequency characterization of on-chip digital interconnects** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
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- **Exploiting CMOS reverse interconnect scaling in multigigahertz amplifier and oscillator design (vol 36, pg 1480, 2001)** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
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- **Near Speed-of-Light On-Chip Electrical Interconnect**
  Chang, R., Yue, C., Wong, S.
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  Kleveland, B., Diaz, C. H., Vook, D., Madden, L., Lee, T. H., Wong, S. S.
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- **A 0dB-IL, 2140 +/- 30 MHz bandpass filter utilizing Q-enhanced spiral inductors in standard CMOS** *Symposium on VLSI Circuits*
  Soorapanth, T., Wong, S. S.

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  Lee, H., Lopatin, S.., Marshall, A., Wong, S.
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  Lee, T. H., Wong, S. S.
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- **Distributed ESD protection for high-speed integrated circuits** *IEEE ELECTRON DEVICE LETTERS*
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- **Quantitative Projections of Reliability and Performance for Low-k/Cu Interconnect Systems**
  Banerjee, K., Kim, D., Amerasekera, A., Hu, C., Goodson, K., Wong, S.
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- **Kinetics of copper drift in low-kappa polymer interlevel dielectrics** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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