

Stanford



S Simon Wong

Professor of Electrical Engineering, Emeritus

CONTACT INFORMATION

• Administrative Contact

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Bio

BIO

Wong studies the fabrication and design of high-performance integrated circuits. His work focuses on understanding and overcoming the limitations of circuit performance imposed by device and technology.

ACADEMIC APPOINTMENTS

- Emeritus (Active) Professor, Electrical Engineering
- Member, Bio-X
- Member, Wu Tsai Neurosciences Institute

HONORS AND AWARDS

- Fellow, IEEE

BOARDS, ADVISORY COMMITTEES, PROFESSIONAL ORGANIZATIONS

- Adviser, Atheros Qualcomm (1998 - 2018)
- Board Director, Pericom Semiconductor (2006 - 2015)

PROFESSIONAL EDUCATION

- PhD, UC Berkeley (1983)

Research & Scholarship

CURRENT RESEARCH AND SCHOLARLY INTERESTS

Current research focuses on

Resistive Random Access Memory (RRAM) and Integration with CMOS

Energy Efficient Approximate Computing for Machine Learning

Teaching

COURSES

2021-22

- Circuits I: EE 101A (Win)
- Circuits II: EE 101B (Spr)

STANFORD ADVISEES

Doctoral Dissertation Reader (AC)

George Alexopoulos, Wei-Chen Chen, Xiangjin Wu, Joon Yang

Master's Program Advisor

Isabela David Rodrigues

Publications

PUBLICATIONS

- **Enhanced Switching Reliability of Hf_{0.5}Zr_{0.5}O₂ Ferroelectric Films Induced by Interface Engineering.** *ACS applied materials & interfaces*
Huang, F., Saini, B., Yu, Z., Yoo, C., Thampy, V., He, X., Baniecki, J. D., Tsai, W., Meng, A. C., McIntyre, P. C., Wong, S.
2023
- **First Observation of Ultra-high Polarization (~ 108 $\mu\text{C}/\text{cm}^2$) in Nanometer Scaled High Performance Ferroelectric HZO Capacitors with Mo Electrodes** *IEEE Symposium on VLSI Technology and Circuits*
Huang, F., Saini, B., Wan, L., Lu, H., He, X., Qin, S., Tsai, W., Gruverman, A., Meng, A., Wong, H., McIntyre, P., Wong, S.
2023
- **Foundry Monolithic 3D BEOL Transistor + Memory Stack: Iso-performance and Iso-footprint BEOL Carbon Nanotube FET+RRAM vs. FEOL Silicon FET+RRAM** *IEEE Symposium on VLSI Technology and Circuits*
Srimani, T., Yu, C., Radway, R., Rich, D., Nelson, M., Wong, S., Murphy, D., Fuller, S., Hills, g., Mitra, S., Shulaker, M.
2023
- **Measurement of Ferroelectric Properties of Nanometer Scaled Individual Metal/Hf_{0.5}Zr_{0.5}O₂/Metal Capacitors** *IEEE ELECTRON DEVICE LETTERS*
Huang, F., Passlack, M., Liew, S., Yu, Z., Lin, Q., Babadi, A., Hou, V., McIntyre, P. C., Wong, S.
2022; 43 (2): 212-215
- **4 Bits/cell Hybrid 1F1R for High Density Embedded Non-Volatile Memory and its Application for Compute in Memory** *IEEE Symposium on VLSI Technology and Circuits*
Chen, W., Huang, F., Qin, S., Yu, Z., Lin, Q., McIntyre, P., Wong, S., Wong, H.
2022
- **8-Layer 3D Vertical Ru/AlOxNy/TiN RRAM with Mega-# Level LRS for Low Power and Ultrahigh-density Memory** *IEEE Symposium on VLSI Technology and Circuits*
Qin, S., Tung, M., Belliveau, E., Liu, S., Kwon, J., Chen, W., Jiang, Z., Wong, S., Wong, H.
2022
- **RADAR: A Fast and Energy-Efficient Programming Technique for Multiple Bits-Per-Cell RRAM Arrays** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Le, B. Q., Levy, A., Wu, T. F., Radway, R. M., Hsieh, E., Zheng, X., Nelson, M., Raina, P., Wong, H., Wong, S., Mitra, S.
2021; 68 (9): 4397-4403
- **3-D Vertical via Nitrogen-Doped Aluminum Oxide Resistive Random-Access Memory** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Lien, Y., Wu, T., Wong, S.
2021; 68 (6): 2712-2716

- **A FORMing-Free HfO₂/HfON-Based Resistive-Gate Metal-Oxide-Semiconductor Field-Effect-Transistor (RG-MOSFET) Nonvolatile Memory With 3-Bit-Per-Cell Storage Capability** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Hsieh, E. R., Chen, K. T., Chen, P. Y., Wong, S. S., Chung, S. S.
2021; 68 (6): 2699-2704
- **Four-Bits-Per-Memory One-Transistor-and-Eight-Resistive-Random-Access-Memory (1T8R) Array** *IEEE ELECTRON DEVICE LETTERS*
Hsieh, E. R., Zheng, X., Le, B. Q., Shih, Y. C., Radway, R. M., Nelson, M., Mitra, S., Wong, S.
2021; 42 (3): 335–38
- **Deep COVID DeteCT: an international experience on COVID-19 lung detection and prognosis using chest CT.** *NPJ digital medicine*
Lee, E. H., Zheng, J. n., Colak, E. n., Mohammadzadeh, M. n., Houshmand, G. n., Bevins, N. n., Kitamura, F. n., Altinmakas, E. n., Reis, E. P., Kim, J. K., Klochko, C. n., Han, M. n., Moradian, et al
2021; 4 (1): 11
- **Bidirectional Analog Conductance Modulation for RRAM-Based Neural Networks** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Jiang, Z., Wang, Z., Zheng, X., Fong, S. W., Qin, S., Chen, H., Ahn, E. C., Cao, J., Nishi, Y., Wong, S., Wong, H.
2020; 67 (11): 4904–10
- **A shallow convolutional neural network predicts prognosis of lung cancer patients in multi-institutional computed tomography image datasets** *Nature Machine Intelligence*
Mukherjee, P., Zhou, M., Lee, E., Schicht, A., Balagurunathan, Y., Napel, S., Gillies, R., Wong, S., Thieme, A., Leung, A., Gevaert, O.
2020; 2 (5): 274–282
- **Next-Generation Ultrahigh-Density 3-D Vertical Resistive Switching Memory (VRSM)-Part I: Accurate and Computationally Efficient Modeling** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Qin, S., Jiang, Z., Li, H., Fujii, S., Lee, D., Wong, S., Wong, H.
2019; 66 (12): 5139–46
- **Next-Generation Ultrahigh-Density 3-D Vertical Resistive Switching Memory (VRSM)-Part II: Design Guidelines for Device, Array, and Architecture** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Jiang, Z., Qin, S., Li, H., Fujii, S., Lee, D., Wong, S., Wong, H.
2019; 66 (12): 5147–54
- **DATASET CULLING: TOWARDS EFFICIENT TRAINING OF DISTILLATION-BASED DOMAIN SPECIFIC MODELS**
Yoshioka, K., Lee, E., Wong, S., Horowitz, M., IEEE
IEEE.2019: 3237–41
- **A Novel Architecture to Build Ideal-linearity Neuromorphic Synapses on a Pure Logic FinFET Platform Featuring 2.5ns PGM-time and 10(12) Endurance**
Hsieh, E. R., Chang, H. Y., Chung, S. S., Chen, T. P., Huang, S. A., Chen, T. J., Cheng, O., Wong, S., IEEE
IEEE.2019: T138–T139
- **High-Density Multiple Bits-per-Cell 1T4R RRAM Array with Gradual SET/RESET and its Effectiveness for Deep Learning**
Hsieh, E. R., Giordano, M., Hodson, B., Levy, A., Osekowsky, S. K., Radway, R. M., Shih, Y. C., Wan, W., Wu, T. F., Zheng, X., Nelson, M., Le, B. Q., Wong, et al
IEEE.2019
- **Deep learning to predict survival prognosis for patients with non-small cell lung cancer using images and clinical data**
Lee, E. H., Zhou, M., Gamboa, N., Brennan, K., Itakura, H., Nair, V., Napel, S., Wong, S., Gevaert, O.
AMER ASSOC CANCER RESEARCH.2018
- **Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM**
Jiang, Z., Qin, S., Li, H., Fujii, S., Lee, D., Wong, S., Wong, H., IEEE
IEEE.2018: 107–8
- **Fault-Tolerant FPGA with Column-Based Redundancy and Power Gating Using RRAM** *IEEE TRANSACTIONS ON COMPUTERS*
Lee, K., Wong, S. S.
2017; 66 (6): 946-956
- **Analysis and Design of a Passive Switched-Capacitor Matrix Multiplier for Approximate Computing** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
Lee, E. H., Wong, S. S.

2017; 52 (1): 261-271

● **LOGNET: ENERGY-EFFICIENT NEURAL NETWORKS USING LOGARITHMIC COMPUTATION**

Lee, E. H., Miyashita, D., Chai, E., Murmann, B., Wong, S., IEEE
IEEE.2017: 5900–5904

● **TPAD: Hardware Trojan Prevention and Detection for Trusted Integrated Circuits** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*

Wu, T. F., Ganesan, K., Hu, Y. A., Wong, H. P., Wong, S., Mitra, S.
2016; 35 (4): 521-534

● **A Deep Learning Framework to Predict Survival from Medical Images of Lung Cancer Patients** *Conference on Neural Information Processing Systems, Workshop on Machine Learning for Health*

Lee, E., Zhou, M., Grove, O., Balagurunathan, Y., Echegaray, S., Gillies, R., Gamboa, N., Murmann, B., Napel, S., Wong, S., Gevaert, O.
2016

● **Switch Application in FPGA** *RESISTIVE SWITCHING: FROM FUNDAMENTALS OF NANOIONIC REDOX PROCESSES TO MEMRISTIVE DEVICE APPLICATIONS*

Sakamoto, T., Wong, S., Liauw, Y., Ielmini, D., Waser, R.
2016: 695-713

● **Fault-tolerant FPGA with Column-based Redundancy and Power Gating Using RRAM**

Lee, K., Wong, S., IEEE
IEEE.2016: 409–14

● **A 2.5GHz 7.7TOPS/W Switched-Capacitor Matrix Multiplier with Co-designed Local Memory in 40nm**

Lee, E. H., Wong, S., IEEE
IEEE.2016: 418–U587

● **Monolithic 3-D FPGAs** *PROCEEDINGS OF THE IEEE*

Zhang, Z., Liauw, Y. Y., Chen, C., Wong, S. S.
2015; 103 (7): 1197-1210

● **Compact One-Transistor-N-RRAM Array Architecture for Advanced CMOS Technology** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*

Yeh, C. S., Wong, S. S.
2015; 50 (5): 1299-1309

● **All-Metal-Nitride RRAM Devices** *IEEE ELECTRON DEVICE LETTERS*

Zhang, Z., Gao, B., Fang, Z., Wang, X., Tang, Y., Sohn, J., Wong, H. P., Wong, S. S., Lo, G.
2015; 36 (1): 29-31

● **FACTORIZATION FOR ANALOG-TO-DIGITAL MATRIX MULTIPLICATION**

Lee, E. H., Udell, M., Wong, S., IEEE
IEEE.2015: 1061–65

● **The Role of Ti Capping Layer in HfOx-Based RRAM Devices** *IEEE ELECTRON DEVICE LETTERS*

Fang, Z., Wang, X. P., Sohn, J., Weng, B. B., Zhang, Z. P., Chen, Z. X., Tang, Y. Z., Lo, G., Provine, J., Wong, S. S., Wong, H. P., Kwong, D.
2014; 35 (9): 912-914

● **Current Conduction Mechanism of Nitrogen-Doped AlOx RRAM** *IEEE TRANSACTIONS ON ELECTRON DEVICES*

Kim, W., Park, S. I., Zhang, Z., Wong, S.
2014; 61 (6): 2158-2163

● **Low-Temperature Monolithic Three-Layer 3-D Process for FPGA** *IEEE ELECTRON DEVICE LETTERS*

Zhang, Z., Chen, C., Crnogorac, F., Chen, S., Griffin, P. B., Pease, R. F., Plummer, J. D., Wong, S. S.
2013; 34 (8): 1044-1046

● **Nanometer-Scale HfOx RRAM** *IEEE ELECTRON DEVICE LETTERS*

Zhang, Z., Wu, Y., Wong, H. P., Wong, S. S.
2013; 34 (8): 1005-1007

- **Impact of III-V and Ge Devices on Circuit Performance** *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS*
Park, J., Oh, S., Kim, S., Wong, H. P., Wong, S. S.
2013; 21 (7): 1189-1200
- **Effect of Wordline/Bitline Scaling on the Performance, Energy Consumption, and Reliability of Cross-Point Memory Array** *ACM JOURNAL ON EMERGING TECHNOLOGIES IN COMPUTING SYSTEMS*
Liang, J., Yeh, S., Wong, S. S., Wong, H. P.
2013; 9 (1)
- **Trusted Integrated Chips Integrating Non-Volatile Memory with CMOS**
Provine, J., Wong, H., Wong, S., Mitra, S.
2013
- **First Demonstration of RRAM Patterned by Block Copolymer Self-Assembly** *IEEE International Electron Devices Meeting (IEDM)*
Wu, Y., Yi, H., Zhang, Z., Jiang, Z., Sohn, J., Wong, S., Wong, H. P.
IEEE.2013
- **Characterization of Geometric Leakage Current of GeO₂ Isolation and Effect of Forming Gas Annealing in Germanium p-n Junctions** *IEEE ELECTRON DEVICE LETTERS*
Jung, W., Park, J., Lin, J. J., Wong, S., Saraswat, K. C.
2012; 33 (11): 1520-1522
- **A superheterodyne receiver front-end with on-chip automatically Q-tuned notch filters** *ANALOG INTEGRATED CIRCUITS AND SIGNAL PROCESSING*
Chi, B., Wang, Z., Wong, S. S.
2012; 71 (3): 453-463
- **Nonvolatile 3D-FPGA with Monolithically Stacked RRAM-Based Configuration Memory**
Yang-Liau, Y., Zhang, Z., Kim, W., El-Gamal, A., Wong, S.
2012
- **Scaling Challenges for the Cross-point Resistive Memory Array to Sub-10nm Node - An Interconnect Perspective** *4th IEEE International Memory Workshop (IMW)*
Liang, J., Yeh, S., Wong, S. S., Wong, H. P.
IEEE.2012
- **Scaling Challenges for the Cross-point Resistive Memory Array to the Single-digit-nm Node – An Interconnect Perspective**
Liang, S., Yip, S., Wong, H., S., Wong, P.
2012
- **Array Architecture for a Nonvolatile 3-Dimensional Cross-Point Resistance-Change Memory** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
Ou, E., Wong, S. S.
2011; 46 (9): 2158-2170
- **A 65 nm CMOS fully-integrated dynamic reconfigurable differential power amplifier with high gain in both bands** *MICROELECTRONICS JOURNAL*
Chi, B., Omid-Zohoor, K., Wang, Z., Wong, S. S.
2011; 42 (6): 855-862
- **A 60GHz Digitally Controlled RF Beamforming Array in 65nm CMOS with Off-Chip Antennas**
Lin, S., Ng, K., Wong, H., Luk, K., Wong, S., Poon, A.
2011
- **Forming-Free Nitrogen-Doped AlO_x RRAM with Sub- μ A Programming Current**
Kim, W., Park, S., I., Zhang, Z., Yang-Liau, Y., Sekar, D., Wong, H., S. P.
2011
- **3D Field Programmable Gate Array**
Yang-Liau, Y., Crnororac, F., Chen, E., Jung, W., Kim, W., Park, S., Wong, S. S.
2011
- **Semiconductor crystal islands for three-dimensional integration** *54th International Conference on Electron, Ion and Photon Beam Technology and Nanofabrication*

Crnogorac, F., Wong, S., Pease, R. F.

A V S AMER INST PHYSICS.2010: C6P53-C6P58

- **Leakage Current Analysis of Lateral p+/n Ge Based Diode Activated at Low Temperature for Three-Dimensional Integrated Circuit (3D-ICs)**
Jung, W., Park, J., Kuzum, D., Kim, W., Wong, S., Saraswat, K.
2010
- **Leakage Current Analysis of Lateral p+/n Ge Based Diode Activated at Low Temperature for Three-Dimensional Integrated Circuit (3D-ICs)** *Symposium on Processing, Materials, and Integration of Damascene and 3D Interconnects held during the 218th Meeting of the Electrochemical-Society*
Jung, W. S., Park, J., Kuzum, D., Kim, W., Wong, S., Saraswat, K. C.
ELECTROCHEMICAL SOC INC.2010: 35–39
- **Optimization of Driver Preemphasis for On-Chip Interconnects** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS*
Bai, Y., Wong, S. S.
2009; 56 (9): 2033-2041
- **RESET Mechanism of TiOx Resistance-Change Memory Device** *IEEE ELECTRON DEVICE LETTERS*
Wang, W., Fujita, S., Wong, S. S.
2009; 30 (7): 733-735
- **Elimination of Forming Process for TiOx Nonvolatile Memory Devices** *IEEE ELECTRON DEVICE LETTERS*
Wang, W., Fujita, S., Wong, S. S.
2009; 30 (7): 763-765
- **Reduction of Inductive Crosstalk Using Quadrupole Inductors** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
Poon, A., Chang, A., Samavati, H., Wong, S. S.
2009; 44 (6): 1756-1764
- **Pi Coil: A New Element for Bandwidth Extension** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II-EXPRESS BRIEFS*
Lin, S., Huang, D., Wong, S.
2009; 56 (6): 454-458
- **A 60-GHz LOW-NOISE AMPLIFIER FOR 60-GHz DUAL-CONVERSION RECEIVER** *MICROWAVE AND OPTICAL TECHNOLOGY LETTERS*
Lin, Y., Wong, S. S.
2009; 51 (4): 885-891
- **The Prospect of 3D-IC** *IEEE Custom Integrated Circuits Conference*
Wong, S. S., El Gamal, A.
IEEE.2009: 445–448
- **Low-Power 48-GHz CMOS VCO and 60-GHz CMOS LNA for 60-GHz Dual-Conversion Receiver** *2009 INTERNATIONAL SYMPOSIUM ON VLSI DESIGN, AUTOMATION AND TEST (VLSI-DAT), PROCEEDINGS OF TECHNICAL PROGRAM*
Lin, Y., Chang, T., Chen, C., Chen, C., Yang, H., Wong, S. S.
2009: 88-?
- **Low-Power 48-GHz CMOS VCO and 60-GHz CMOS LNA for 60-GHz Dual-Conversion Receiver**
Lin, Y., Chang, T., Chen, C., Chen, C., Yang, H., Wong, S.
2009
- **Performance Comparison between Capacitively Driven Low Swing and Conventional Interconnects for Cu and Carbon Nanotube Wire Technologies** *IEEE International Interconnect Technology Conference*
Koo, K., Kapur, P., Park, J., Noh, H., Wong, S. S., Saraswat, K. C.
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- **A High-Performance 3D-SRAM Architecture**
Wong, S., Nho, H.
2009
- **Numerical estimation of yield in sub-100-nm SRAM design using Monte Carlo simulation** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II-EXPRESS BRIEFS*
Nho, H., Yoon, S., Wong, S. S., Jung, S.

2008; 55 (9): 907-911

- **High-performance gate-all-around GeOI p-MOSFETs fabricated by rapid melt growth using plasma nitridation and ALD Al₂O₃ gate dielectric and self-aligned NiGe contacts** *IEEE ELECTRON DEVICE LETTERS*
Feng, J., Thareja, G., Kobayashi, M., Chen, S., Poon, A., Bai, Y., Griffin, P. B., Wong, S. S., Nishi, Y., Plummer, J. D.
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- **A High-speed, Low-power 3D-SRAM Architecture** *IEEE Custom Integrated Circuits Conference*
Nho, H. H., Horowitz, M., Wong, S. S.
IEEE.2008: 201-204
- **A low-power V-band CMOS low-noise amplifier using current-sharing technique**
Yang, H., Lin, Y., Chen, C., Wong, S. S., IEEE
IEEE.2008: 964+
- **A Low-Power V-Band CMOS Low Noise Amplifier using Current Sharing Technique**
Yang, H., Lin, Y., Chen, C., Wong, S.
2008
- **Monolithic 3D Integrated Circuits**
Wong, S., El-Gamal, A., Griffin, P., Nishi, Y., Pease, F., Plummer, J.
2008
- **An on-chip dipole antenna for millimeter-wave transmitters** *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*
Park, P. H., Wong, S. S.
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- **Thickness and stoichiometry dependence of the thermal conductivity of GeSbTe films** *APPLIED PHYSICS LETTERS*
Reifenberg, J. P., Panzer, M. A., Kim, S., Gibby, A. M., Zhang, Y., Wong, S., Wong, H. P., Pop, E., Goodson, K. E.
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- **Closed-form RC and RLC delay models considering input rise time** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS*
Kim, S., Wong, S. S.
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- **Statistical simulation methodology for sub100 nm memory design** *ELECTRONICS LETTERS*
Nho, H., Yoon, S., Wong, S., Jung, S.
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- **Performance benefits of monolithically stacked 3-D FPGA** *International Symposium on Field-Programmable Gate Arrays*
Lin, M., El Gamal, A., Lu, Y., Wong, S.
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- **Resistive switching mechanism in ZnxCd1-xS nonvolatile memory devices** *IEEE ELECTRON DEVICE LETTERS*
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- **A superheterodyne receiver front-end with on-chip automatically Q-tuned notch filters** *2007 IEEE RADIO FREQUENCY INTEGRATED CIRCUITS (RFIC) SYMPOSIUM, DIGEST OF PAPERS*
Chi, B., Wang, Z., Wong, S. S.
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Lin, M., El Gamal, A., Lu, Y., Wong, S.
2006
 - **Multiphysics modeling and impact of thermal boundary resistance in phase change memory devices** *10th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*
Reifenberg, J., Pop, E., Gibby, A., Wong, S., Goodson, K.
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 - **Integrated transformer baluns for RF low noise and power amplifiers** *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*
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 - **Analysis and synthesis of on-chip spiral inductors** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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2005; 52 (2): 176-182
 - **Scalability of RF CMOS** *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*
Yue, C. P., Wong, S. S.
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 - **Studies of the driving force for room-temperature microstructure evolution in electroplated copper films** *JOURNAL OF VACUUM SCIENCE & TECHNOLOGY B*
Lee, H., Nix, W. D., Wong, S. S.
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Talwalkar, N. A., Yue, C. P., Gan, H. T., Wong, S. S.
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Lai, T. L., Wong, S. P.
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Chang, R. T., Yang, M. T., Ho, P. P., Wang, Y. J., Chia, Y. T., Liew, B. K., Yue, C. P., Wong, S. S.
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 - **A 10-GHz global clock distribution using coupled standing-wave oscillators** *IEEE International Solid-State Circuits Conference*
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Soorapanth, T., Wong, S. S.
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