



Jian Chen

Adjunct Professor, Electrical Engineering

Bio

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Retired executive with 30 years of experience in NOR, 2D NAND and 3D NAND flash memories, in the areas of device physics, process integration, reliability, test & product engineering, memory systems architecture, eco-systems and new business development. With a passion for innovation and practical solutions and teamwork, built multiple teams from ground up including at international sites.

Inventor of >150 US patents and some significant ideals that have been used in over 10 generations of NAND memory chip and systems, such as binary cache for MLC (USP# 5,930,167), fast MLC NAND writing method GPW (USP# 6,522,580 and 6,643,188), read method to correct cell to cell coupling effect (USP#5,867,429), NAND memory WL air-gap (USP# 7,045,849), and highly reliable systems EPWR (USP#8,214,700, 8,386,861 aka EPWR).

Published the paper that coined the term GIDL, and the first paper that identified the physics of the GIDL current as due to band-to-band tunneling.

Google scholar h-index 57.