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Publications

PUBLICATIONS

- **A 52-Gb/s Sub-1-pJ/bit PAM4 Receiver in 40-nm CMOS for Low-Power Interconnects** *IEEE Open Journal of Circuits and Systems*
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- **A 32-Gb/s 0.46-pJ/bit PAM4 CDR Using a Quarter-Rate Linear Phase Detector and a Self-Biased PLL-Based Multiphase Clock Generator** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Zhang, Z., Zhu, G., Wang, C., Wang, L., Yue, C.
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- **A 52-Gb/s Sub-1pJ/bit PAM4 Receiver in 40-nm CMOS for Low-Power interconnects**
  Wang, C., Zhu, G., Zhang, Z., Yue, C., IEEE
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- **Compact Modeling of Laser Diode for Visible Laser Light Communication (VLLC)Systems** *Conference on Lasers and Electro-Optics Pacific Rim (CLEO-PR)*
  WANG, C., et al
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- **A 16-GB/S 0-DB Power Back-Off 16-QAM Transmitter at 28 GHZ in 65-NM CMOS** *IEEE Symposium on VLSI Circuits*
  MENG, X., WANG, C., Kalantari, M., YUE, C. P.
  2018