



Po-Han Chen

Ph.D. Student in Electrical Engineering, admitted Winter 2021

Bio

BIO

Po-Han Chen is an EE Ph.D. student at Stanford University supervised by Prof. Priyanka Raina. He received his B.S. in Electrical Engineering and Computer Science (EECS) and M.S. in Electrical Engineering from National Tsing Hua University (Taiwan) in 2016 and 2018 respectively. Before joining Stanford, he was a digital circuit designer at MediaTek where he worked on developing hardware architectures of image processing pipeline. He is interested in designing hardware accelerators. Most of his previous works were related to computational photography algorithms such as digital refocusing. Currently, He is focusing on analyzing and designing architecture of CGRAs to create high-performance, energy-efficient, and reconfigurable computing platforms.

Publications

PUBLICATIONS

- **Amber: A 16-nm System-on-Chip With a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
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- **AHA: An Agile Approach to the Design of Coarse-Grained Reconfigurable Accelerators and Compilers** *ACM Transactions on Embedded Computing Systems*
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- **A 250-mW 5.4G-Rendered-Pixel/s Realistic Refocusing Processor for High-Performance Five-Camera Mobile Devices** *IEEE OPEN JOURNAL OF THE SOLID-STATE CIRCUITS SOCIETY*
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- **An Open-Source 4x8 Coarse-Grained Reconfigurable Array Using SkyWater 130 nm Technology and Agile Hardware Design Flow**
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- **mflowgen: a modular flow generator and ecosystem for community-driven physical design** *DAC '22: Proceedings of the 59th ACM/IEEE Design Automation Conference*
Carsello, A., Thomas, J., Nayak, A., Chen, P., Horowitz, M., Raina, P., Torng, C.
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- **SAPIENS: A 64-kb RRAM-Based Non-Volatile Associative Memory for One-Shot Learning and Inference at the Edge** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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