Stanford

Po-Han Chen

- Ph.D. Student in Electrical Engineering, admitted Winter 2021
- Masters Student in Electrical Engineering, admitted Winter 2022

Bio

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Po-Han Chen is an EE Ph.D. student at Stanford University supervised by Prof. Priyanka Raina. He received his B.S. in Electrical Engineering and Computer Science (EECS) and M.S. in Electrical Engineering from National Tsing Hua University (Taiwan) in 2016 and 2018 respectively. Before joining Stanford, he was a digital circuit designer at MediaTek where he worked on developing hardware architectures of image processing pipeline. He is interested in designing hardware accelerators. Most of his previous works were related to computational photography algorithms such as digital refocusing. Currently, He is focusing on analyzing and designing architecture of CGRAs to create high-performance, energy-efficient, and reconfigurable computing platforms.

Publications

PUBLICATIONS

- **SAPIENS: A 64-kb RRAM-Based Non-Volatile Associative Memory for One-Shot Learning and Inference at the Edge** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Li, H., Chen, W., Levy, A., Wang, C., Wang, H., Chen, P., Wan, W., Khwa, W., Chuang, H., Chih, Y., Chang, M., Wong, H., Raina, et al
  2021; 68 (12): 6637-6643