Stanford

Kalhan Koul

Ph.D. Student in Electrical Engineering, admitted Autumn 2019

Bio

BIO

Kalhan Koul is an EE Ph.D. student at Stanford University supervised by Prof. Priyanka Raina. Previously, he was a Digital Design Intern at Micron and Silicon Labs. He received a B.S. in Electrical Engineering Honors and a B.A. in Plan II Honors (Liberal Arts) from The University of Texas in 2018 and his M.S. in Electrical Engineering from Stanford University in 2021. During his PhD he has worked on three chip tapeouts. The first was Chimera, a DNN accelerator utilizing RRAM for low energy inference. The next was Amber, a coarse grained reconfigurable array (CGRA) optimized for image processing and machine learning applications. Finally, Kalhan led the tapeout of Onyx, a CGRA accelerating both dense and sparse kernels on the same fabric. His current research focuses on further improving the efficiency of the CGRA and extending its acceleration to end-to-end machine learning workloads.

Publications

PUBLICATIONS

- **AHA: An Agile Approach to the Design of Coarse-Grained Reconfigurable Accelerators and Compilers** *ACM Transactions on Embedded Computing Systems*
  Koul, K., Melchert, J., Sreedhar, K., Truong, L., Nyengele, G., Zhang, K., Liu, Q., Setter, J., Chen, P., Mei, Y., Strange, M., Daly, R., Donovick, et al
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- **CHIMERA: A 0.92-TOPS, 2.2-TOPS/W Edge AI Accelerator With 2-MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Prabhu, K., Gural, A., Khan, Z. F., Radway, R. M., Giordano, M., Koul, K., Doshi, R., Kustin, J. W., Liu, T., Lopes, G. B., Turbiner, V., Khwa, W., Chih, et al
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