Stanford

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Bio

BIO

Kavya is an electrical engineering PhD student advised by Mark Horowitz. She is interested in architecture design and developing hardware accelerators for machine learning and cryptography applications. Her current research explores how to efficiently accelerate the extended GCD computation for verifiable delay functions and modular inversion in cryptography. She previously worked with the Agile Hardware (AHA) Project in developing Lake, a parameterizable memory generator that can be configured at runtime to support different image processing and machine learning applications. She is supported by Stanford's Knight-Hennessy scholarship and received her B.S. in electrical engineering and BEM (Business, Economics, & Management) from Caltech in 2019 and her M.S. in electrical engineering from Stanford in 2021.

LINKS

- https://sites.google.com/view/kavyasreedhar/home: https://sites.google.com/view/kavyasreedhar/home

Publications

PUBLICATIONS

- **Creating an Agile Hardware Design Flow**
  Bahr, R., Barrett, C., Bhagdikar, N., Carsello, A., Daly, R., Donovick, C., Durst, D., Fatahalian, K., Feng, K., Hanrahan, P., Hofstee, T., Horowitz, M., Huff, et al
  IEEE.2020