Stanford

Kavya Sreedhar

Ph.D. Student in Electrical Engineering, admitted Autumn 2019

Bio

BIO

Kavya Sreedhar is an electrical engineering PhD candidate advised by Mark Horowitz. Her research interests include architecture design and developing hardware accelerators for cryptography and machine learning applications. On the cryptography side, she has worked on designing a fast extended GCD accelerator for constant-time modular inversion and verifiable delay functions. On the deep learning side, she is working on dynamically adapting the execution of state-of-the-art models for use in real-time systems and accelerating dynamic transformer models for computer vision in an ongoing collaboration with NVIDIA. She previously worked with the Agile Hardware (AHA) Project in developing Lake, a parameterizable memory generator that can be configured at runtime to support different image processing and machine learning applications. As part of her research, she has worked on taping out three chips in SKY130nm, GF12nm, and TSMC16nm. Kavya is supported by the Quad Fellowship (2023 to 2024) and Stanford's Knight-Hennessy Graduate Fellowship (2019 to 2022). She received a B.S. in Electrical Engineering and BEM (Business, Economics, & Management) from Caltech in 2019 and a M.S. in Electrical Engineering from Stanford in 2021.

EDUCATION AND CERTIFICATIONS

- M.S., Stanford University , Electrical Engineering (2021)
- B.S., California Institute of Technology , Business, Economics, and Management (2019)
- B.S., California Institute of Technology , Electrical Engineering (2019)

LINKS

- Personal Website: https://bit.ly/kavyasreedhar

Publications

PUBLICATIONS

- **AHA: An Agile Approach to the Design of Coarse-Grained Reconfigurable Accelerators and Compilers** *ACM Transactions on Embedded Computing Systems*
  Koul, K., Melchert, J., Sreedhar, K., Truong, L., Nyengele, G., Zhang, K., Liu, Q., Setter, J., Chen, P., Mei, Y., Strange, M., Daly, R., Donovick, et al
  2023; 22 (2)
- **Creating an Agile Hardware Design Flow**
  Bahr, R., Barrett, C., Bhagdikar, N., Carsello, A., Daly, R., Donovick, C., Durst, D., Fatahalian, K., Feng, K., Hanrahan, P., Hofstee, T., Horowitz, M., Huff, et al
  IEEE.2020