

Stanford

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Ph.D. Student in Electrical Engineering, admitted Autumn 2019

Publications

PUBLICATIONS

- **Thermal Scaffolding for Ultra-Dense 3D Integrated Circuits**

Rich, D., Kasperovich, A., Malakoutian, M., Radway, R. M., Hagiwara, S., Yoshikawa, T., Chowdhury, S., Mitra, S., IEEE
IEEE.2023

- **EMBER: Efficient Multiple-Bits-Per-Cell Embedded RRAM Macro for High-Density Digital Storage** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*

Levy, A., Upton, L. R., Scott, M. D., Rich, D., Khwa, W., Chih, Y., Chang, M., Mitra, S., Murmann, B., Raina, P.
2024

- **Cooling future system-on-chips with diamond inter-tiers** *CELL REPORTS PHYSICAL SCIENCE*

Malakoutian, M., Kasperovich, A., Rich, D., Woo, K., Perez, C., Soman, R., Saraswat, D., Kim, J., Noshin, M., Chen, M., Vaziri, S., Bao, X., Shih, et al
2023; 4 (12)

- **EMBER: A 100 MHz, 0.86 mm², Multiple-Bits-per-Cell RRAM Macro in 40 nm CMOS with Compact Peripherals and 1.0 pJ/bit Read Circuitry**

Upton, L. R., Levy, A., Scott, M. D., Rich, D., Khwa, W., Chih, Y., Chang, M., Mitra, S., Raina, P., Murmann, B., IEEE
IEEE.2023: 469-472

- **Ultra-Dense 3D Physical Design Unlocks New Architectural Design Points with Large Benefits**

Srimani, T., Radway, R. M., Kim, J., Prabhu, K., Rich, D., Gilardi, C., Raina, P., Shulaker, M., Lim, S., Mitra, S., IEEE
IEEE.2023

- **Testbench on a Chip: A Yield Test Vehicle for Resistive Memory Devices**

Upton, L. R., Lallement, G., Scott, M. D., Taylor, J., Radway, R. M., Rich, D., Nelson, M., Mitra, S., Murmann, B., IEEE
IEEE.2023: 576-582