Stanford

Oyekunle Olukotun

Cadence Design Systems Professor and Professor of Electrical Engineering

CONTACT INFORMATION

- **Administrative Contact**

  Dan Moreau - Program Manager

  Email dmoreau@stanford.edu

  Tel (650) 723-1430

Bio

BIO

Kunle Olukotun is the Cadence Design Systems Professor in the School of Engineering and Professor of Electrical Engineering and Computer Science at Stanford University. Olukotun is well known as a pioneer in multicore processor design and the leader of the Stanford Hydra chip multiprocessor (CMP) research project. Olukotun founded Afara Websystems to develop high-throughput, low-power multicore processors for server systems. The Afara multicore processor, called Niagara, was acquired by Sun Microsystems. Niagara derived processors now power all Oracle SPARC-based servers. Olukotun currently directs the Stanford Pervasive Parallelism Lab (PPL), which seeks to proliferate the use of heterogeneous parallelism in all application areas using Domain Specific Languages (DSLs).

ACADEMIC APPOINTMENTS

- Professor, Electrical Engineering
- Professor, Computer Science
- Member, Wu Tsai Neurosciences Institute

HONORS AND AWARDS

- Fellow, ACM (2007)
- Fellow, IEEE (2007)

PROFESSIONAL EDUCATION

- PhD, Michigan (1991)

Teaching

COURSES

2018-19

- Digital Systems Design Lab: EE 109 (Spr)
- Hardware Accelerators for Machine Learning: CS 217 (Aut)
- Parallel Computing: CS 149 (Win)

2017-18

- Digital Systems Design Lab: EE 109 (Spr)
- Parallel Computing: CS 149 (Win)

2016-17

- Digital Systems Design Lab: EE 109 (Spr)
- Parallel Computing: CS 149 (Win)

2015-16

- Digital Systems Architecture: EE 180 (Win)
- Digital Systems Design Lab: EE 109 (Spr)
- Parallel Computing Research Project: CS 315B (Aut)

STANFORD ADVISEES

Postdoctoral Faculty Sponsor

Muhammad Shahbaz

Doctoral Dissertation Advisor (AC)

Tian Zhao

Doctoral (Program)

Taeyoung Kong, Tian Zhao

Publications

PUBLICATIONS

- **Plasticine: A Reconfigurable Architecture For Parallel Patterns** *ISCA '17: 44th International Symposium on Computer Architecture, June 2017*
  Prabhakar, R., Zhang, Y., Koeplinger, D., Feldman, M., Zhao, T., Hadjis, S., Pedram, A., Kozyrakis, C., Olukotun, K.

- **Beyond Parallel Programming with Domain Specific Languages** *ACM SIGPLAN NOTICES*
  Olukotun, K.
  2014; 49 (8): 179-179

- **Delite: A Compiler Architecture for Performance-Oriented Embedded Domain-Specific Languages** *ACM TRANSACTIONS ON EMBEDDED COMPUTING SYSTEMS*
  Sujeeth, A. K., Brown, K. J., Lee, H., Rompf, T., Chafi, H., Odersky, M., Olukotun, K.
  2014; 13

- **Surgical Precision JIT Compilers** *35th ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*
  Rompf, T., Sujeeth, A. K., Brown, K. J., Lee, H., Chafi, H., Olukotun, K.
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- **Forge: Generating a High Performance DSL Implementation from a Declarative Specification** *ACM SIGPLAN NOTICES*
  Sujeeth, A. K., Gibbons, A., Brown, K. J., Lee, H., Rompf, T., Odersky, M., Olukotun, K.
  2014; 49 (3): 145-154

- **Optimizing Data Structures in High-Level Programs New Directions for Extensible Compilers based on Staging** *ACM SIGPLAN NOTICES*
  Rompf, T., Sujeeth, A. K., Amin, N., Brown, K. J., Jovanovic, V., Lee, H., Jonnalagedda, M., Olukotun, K., Odersky, M.
  2013; 48 (1): 497-510

- **High Performance Embedded Domain Specific Languages** *ACM SIGPLAN NOTICES*
  Olukotun, K.
  2012; 47 (9): 139-139

- **Green-Marl: A DSL for Easy and Efficient Graph Analysis** *ACM SIGPLAN NOTICES*
  Hong, S., Chafi, H., Sedlar, E., Olukotun, K.
  2012; 47 (4): 349-362
- **Green-Marl: A DSL for Easy and Efficient Graph Analysis**
  Hong, S., Chafi, H., Sedlar, E., Olukotun, K.
  2012
- **IMPLEMENTING DOMAIN-SPECIFIC LANGUAGES FOR HETEROGENEOUS PARALLEL COMPUTING** *IEEE MICRO*
  Lee, H., Brown, K. J., Sujeeth, A. K., Chafi, H., Olukotun, K., Rompf, T., Odersky, M.
  2011; 31 (5): 42-52
- **Accelerating CUDA Graph Algorithms at Maximum Warp** *ACM SIGPLAN NOTICES*
  Hong, S., Kim, S. K., Oguntebi, T., Olukotun, K.
  2011; 46 (8): 267-276
- **A Domain-Specific Approach To Heterogeneous Parallelism** *ACM SIGPLAN NOTICES*
  Chafi, H., Sujeeth, A. K., Brown, K. J., Lee, H., Atreya, A. R., Olukotun, K.
  2011; 46 (8): 35-45
- **Hardware Acceleration of Transactional Memory on Commodity Systems** *ACM SIGPLAN NOTICES*
  Casper, J., Oguntebi, T., Hong, S., Bronson, N. G., Kozyrakis, C., Olukotun, K.
  2011; 46 (3): 27-38
- **Implementing Domain-Specific Languages for Heterogeneous Parallel Computing** *IEEE Micro: Special Issue on CPU, GPU, and Hybrid Computing*
  Lee, H., Brown, Kevin, J., Sujeeth, Arvind, K., Chafi, H., Rompf, T., Odersky, M., Olukotun, Oyekunle, A.
  2011
- **Hardware Acceleration of Transactional Memory on Commodity Systems**
  Casper, J., Oguntebi, T., Hong, S., Bronson, Nathan, G., Kozyrakis, C., Olukotun, K.
  2011
- **Accelerating CUDA Graph Algorithms at Maximum Warp**
  Hong, S., Kim, S. K., Oguntebi, T., Olukotun, K.
  2011
- **A Domain-Specific Approach to Heterogeneous Parallelism**
  Chafi, H., Sujeeth, Arvind, K., Brown, Kevin, J., Lee, H., Atreya, Anand, R., Olukotun, K.
  2011
- **Building-Blocks for Performance Oriented DSLs**
  Rompf, T., Sujeeth, Arvind, K., Lee, H., Brown, Kevin, J., Chafi, H., Odersky, M., Olukotun, Oyekunle, A.
  2011
- **OptiML: An Implicitly Parallel Domain-Specific Language for Machine Learning**
  Sujeeth, Arvind, K., Lee, H., Brown, Kevin, J., Rompf, T., Chafi, H., Wu, M., Olukotun, Oyekunle, A.
  2011
- **Efficient Parallel Graph Exploration on Multi-Core CPU and GPU**
  Hong, S., Oguntebi, T., Olukotun, K.
  2011
- **A Heterogeneous Parallel Framework for Domain-Specific Languages**
  Brown, Kevin, J., Sujeeth, Arvind, K., Lee, H., Rompf, T., Chafi, H., Odersky, M., Olukotun, Oyekunle, A.
  2011
- **Language Virtualization for Heterogeneous Parallel Computing** *Conference on Object Oriented Programming Systems, Languages and Applications/SPLASH 2010*
  Chafi, H., DeVito, Z., Moors, A., Rompf, T., Sujeeth, A. K., Hanrahan, P., Odersky, M., Olukotun, K.
  ASSOC COMPUTING MACHINERY.2010: 835–47

- **A Practical Concurrent Binary Search Tree** *ACM SIGPLAN NOTICES*
  Bronson, N. G., Casper, J., Chafi, H., Olukotun, K.
  2010; 45 (5): 257-268
- **UBIQUITOUS PARALLEL COMPUTING FROM BERKELEY, ILLINOIS, AND STANFORD** *IEEE MICRO*
  Catanzaro, B., Fox, A., Keutzer, K., Patterson, D., Su, B., Snir, M., Olukotun, K., Hanrahan, P., Chafi, H.
  2010; 30 (2): 41-55
- **A Large-scale Architecture for Restricted Boltzmann Machines**
  Kim, S. K., McMahon, Peter, L., Olukotun, K.
  2010
- **FARM: A Prototyping Environment for Tightly-Coupled, Heterogeneous Architectures**
  Oguntebi, T., Hong, S., Casper, J., Bronson, N., Kozyrakis, C., Olukotun, K.
  2010
- **Implementing and Evaluating Nested Parallel Transactions in Software Transactional Memory**
  Baek, W., Bronson, N., Kozyrakis, C., Olukotun, K.
  2010
- **Transactional Predication: High-Performance Concurrent Sets and Maps for STM**
  Bronson, Nathan, G., Casper, J., Chafi, H., Olukotun, K.
  2010
- **EigenBench: A Simple Exploration Tool for Orthogonal TM Characterisitics**
  Hong, S., Oguntebi, T., Casper, J., Bronson, N., Koyrakis, C., Olukotun, K.
  2010
- **CCSTM: A Library-Based STM for Scala**
  Bronson, Nathan, G., Chafi, H., Olukotun, K.
  2010
- **Making Nested Parallel Transactions Practical using Lightweight Hardware Support**
  Baek, W., Bronson, N., Kozyrakis, C., Olukotun, K.
  2010
- **Language Virtualization for Heterogeneous Parallel Computing**
  Chafi, H., DeVito, Z., Moors, A., Rompf, T., Sujeeth, Arvind, K., Hanrahan, P., Olukotun, Oyekunle, A.
  2010
- **Implementing and Evaluating a Model Checker for Transactional Memory Systems**
  Baek, W., Bronson, Nathan, G., Kozyrakis, C., Olukotun, K.
  2010
- **A Practical Concurrent Binary Search Tree.**
  Bronson, Nathan, G., Casper, J., Chafi, H., Olukotun, K.
  2010
- **A Highly Scalable Restricted Boltzmann Machine FPGA Implementation**
  Kim, S. K., McAfee, Lawrence, C., McMahon, Peter, L., Olukotun, K.
  2009
- **Feedback-Directed Barrier Optimization in a Strongly Isolated STM** *ACM SIGPLAN NOTICES*
  Bronson, N. G., Kozyrakis, C., Olukotun, K.
  2009; 44 (1): 213-225
- **Feedback-Directed Barrier Optimization in a Strongly Isolated STM**
  Bronson, Nathan, G., Kozyrakis, C., Olukotun, K.
  2009

- **Improving Software Concurrency with Hardware-assisted Memory Snapshot** *20th ACM Symposium on Parallelism in Algorithms and Architectures*
  Chung, J., Seo, J., Baek, W., Minh, C. C., McDonald, A., Kozyrakis, C., Olukotun, K.
  ASSOC COMPUTING MACHINERY.2008: 363–363

- **STAMP: Stanford Transactional Applications for Multi-Processing** *IEEE International Symposium on Workload Characterization*
  Minh, C. C., Chung, J., Kozyrakis, C., Olukotun, K.
  IEEE.2008: 31–42

- **ASeD: Availability, Security, and Debugging Support using Transactional Memory** *20th ACM Symposium on Parallelism in Algorithms and Architectures*
  Chung, J., Baek, W., Bronson, N. G., Seo, J., Kozyrakis, C., Olukotun, K.
  ASSOC COMPUTING MACHINERY.2008: 366–366

- **Transactional memory: The hardware-software interface** *IEEE MICRO*
  McDonald, A., Carlstrom, B. D., Chung, J., Minh, C. C., Chafi, H., Kozyrakis, C., Olukotun, K.
  2007; 27 (1): 67-76

- **An Effective Hybrid Transactional Memory System with Strong Isolation Guarantees** *34th Annual International Symposium on Computer Architecture*
  Minh, C. C., Trautmann, M., Chung, J., McDonald, A., Bronson, N., Casper, J., Kozyrakis, C., Olukotun, K.
  ASSOC COMPUTING MACHINERY.2007: 69–80

- **Transactional Collection Classes** *ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*
  Carlstrom, B. D., McDonald, A., Carbin, M., Kozyrakis, C., Olukotun, K.
  ASSOC COMPUTING MACHINERY.2007: 56–67

- **A Practical FPGA-based Framework for Novel CMP Research** *15th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*
  Wee, S., Casper, J., Njoroge, N., Tesylar, Y., Ge, D., Kozyrakis, C., Olukotun, K.
  ASSOC COMPUTING MACHINERY.2007: 116–125

- **Towards Soft Optimization Techniques for Parallel Cognitive Applications** *19th Annual Symposium on Parallelism in Algorithms and Architectures*
  Baek, W., Chung, J., Minh, C. C., Kozyrakis, C., Olukotun, K.
  ASSOC COMPUTING MACHINERY.2007: 59–60

- **A scalable, non-blocking approach to transactional memory** *13th International Symposium on High-Performance Computer Architecture*
  Chafi, H., Casper, J., Carlstrom, B. D., McDonald, A., Minh, C. C., Baek, W., Kozyrakis, C., Olukotun, K.
  IEEE COMPUTER SOC.2007: 97–108

- **ATLAS: A chip-multiprocessor with Transactional Memory support** *Design, Automation and Test in Europe Conference and Exhibition (DATE 07)*
  Njoroge, N., Casper, J., Wee, S., Teslyar, Y., Ge, D., Kozyrakis, C., Olukotun, K.
  IEEE.2007: 3–8

- **Executing Java programs with transactional memory** *OOPSLA Workshop on Synchronization and Concurrent in Object-Oriented Languages*
  Carlstrom, B. D., Chung, J., Chafi, H., McDonald, A., Minh, C. C., Hammond, L., Kozyrakis, C., Olukotun, K.
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- **Tradeoffs in transactional memory virtualization** *ACM SIGPLAN NOTICES*
  Chung, J., Minh, C. C., McDonald, A., Skare, T., Chafi, H., Carlstrom, B. D., Kozyrakis, C., Olukotun, K.
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- **The ATOMO Sigma transactional programming language** *ACM SIGPLAN NOTICES*
  Carlstrom, B. D., McDonald, A., Chafi, H., Chung, J., Minh, C. C., Kozyrakis, C., Olukotun, K.
  2006; 41 (6): 1-13

- **The Atomos Transactional Programming Language**
  Carlstrom, Brian, D., McDonald, A., Chafi, H., Chung, J., Minh, C. C., Kozyrakis, C., Olukotun, Oyekunle, A.
  2006

- **Architectural semantics for practical Transactional Memory** *33rd International Symposium on Computer Architecture*
  McDonald, A., Chung, J., Carlstrom, B. D., Minh, C. C., Chafi, H., Kozyrakis, C., Olukotun, K.
  IEEE COMPUTER SOC.2006: 53–64

- **The common case transactional behavior of multithreaded programs** *12th International Symposium on High-Performance Computer Architecture*
  Chung, J., Chafi, H., Minh, C. C., McDonald, A., Carlstrom, B., Kozyrakis, C., Olukotun, K.
  IEEE COMPUTER SOC.2006: 271–282
- **The Common Case Transactional Behavior of Multithreaded Programs**
  Chung, J., Chafi, H., Minh, C. C., McDonald, A., Carlstrom, Brian, D., Kozyrakis, C., Olukotun, Oyekunle, A.
  2006
- **Architectural Semantics for Practical Transactional Memory**
  McDonald, A., Chung, J., Carlstrom, Brian, D., Minh, C. C., Chafi, H., Kozyrakis, C., Olukotun, Oyekunle, A.
  2006
- **The Software Stack for Transactional Memory: Challenges and Opportunities**
  Carlstrom, Brian, D., Chung, J., Kozyrakis, C., Olukotun, K.
  2006
- **Tradeoffs in Transactional Memory Virtualizations**
  Chung, J., Minh, C. C., McDonald, A., Chafi, H., Carlstrom, Brian, D., Skare, T., Olukotun, Oyekunle, A.
  2006
- **Niagara: A 32-way multithreaded SPARC processor** *IEEE MICRO*
  Kongetira, P., Aingaran, K., Olukotun, K.
  2005; 25 (2): 21-29
- **The Future of Microprocessors** *ACM QUEUE Magazine*
  Olukotun, K., Hammond, L.
  2005
- **Maximizing CMP throughput with mediocre cores** *PACT 2005: 14TH INTERNATIONAL CONFERENCE ON PARALLEL ARCHITECTURES AND COMPILATION TECHNIQUES*
  Davis, J. D., Laudon, J., Olukotun, K.
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- **A new approach to programming and prototyping parallel systems** *HIGH PERFORMANCE COMPUTING - HIPC 2005, PROCEEDINGS*
  Olukotun, K.
  2005; 3769: 4-4
- **Characterization of TCC on chip-multiprocessors** *14th International Conference on Parallel Architectures and Compilation Techniques*
  McDonald, A., Chung, J. W., Chafi, H., Minh, C. C., Carlstrom, B. D., Hammond, L., Kozyrakis, C., Olukotun, K.
  IEEE COMPUTER SOC.2005: 63–74
- **Maximizing CMP Throughput with Mediocre Cores**
  Davis, John, D., Laudon, J., Olukotun, K.
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- **TAPE: A Transactional Application Profiling Environment**
  Chafi, H., Minh, C. C., McDonald, A., Carlstrom, Brian, D., Chung, J., Hammond, L., Olukotun, Oyekunle, A.
  2005
- **Article about Kunle Olukuton's Niagara processor: Sun's Big Splash** *IEEE Spectrum Magazine*
  Olukotun, K., Geppert, L.
  2005
- **Transactional Execution of Java Programs**
  Carlstrom, Brian, D., Chung, J., Chafi, H., McDonald, A., Minh, C. C., Hammond, L., Olukotun, Oyekunle, A.
  2005
- **Exposing Speculative Thread Parallelism in SPEC2000**
  Prabhu, M., Olukotun, K.
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- **Characterization of TCC on Chip-Multiprocessors**
  McDonald, A., Chung, J., Chafi, H., Minh, C. C., Carlstrom, Brian, D., Hammond, L., Olukotun, Oyekunle, A.
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- **Transactional coherence and consistency: Simplifying parallel hardware and software** *IEEE MICRO*
  Hammond, L., Carlstrom, B. D., Wong, V., Chen, M., Kozyrakis, C., Olukotun, K.
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- **Programming with transactional coherence and consistency (TCC)** *11th International Conference on Architectural Support for Programming Languages and Operating Systems*
  Hammond, L., Carlstrom, B. D., Wong, V., Hertzberg, B., Chen, M., Kozyrakis, C., Olukotun, K.
  ASSOC COMPUTING MACHINERY.2004: 1–13

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  Hammond, L., Carlstrom, Brian, D., Wong, V., Chen, M., Kozyrakis, C., Olukotun, K.
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- **Transactional memory coherence and consistency** *31st Annual International Symposium on Computer Architecture*
  Hammond, L., Wong, V., Chen, M., Carlstrom, B. D., Davis, J. D., Hertzberg, B., Prabhu, M. K., Wijaya, H., Kozyrakis, C., Olukotun, K.
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- **Niagara: A 32-Way Multithreaded SPARC Processor** *IEEE MICRO Magazine, March-April 2005, and presented at Hot Chips*
  Kongetira, P., Aingaran, K., Olukotun, K.
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- **Transactional Memory Coherence and Consistency**
  Hammond, L., Wong, V., Chen, M., Hertzberg, B., Carlstrom, Brian, D., Davis, John, D., Olukotun, Oyekunle, A.
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- **Programming with Transactional Coherence and Consistency (TCC)**
  Hammond, L., Carlstrom, Brian, D., Wong, V., Hertzberg, B., Chen, M., Kozyrakis, C., Olukotun, Oyekunle, A.
  2004

- **The Jrpm system for dynamically parallelizing sequential Java programs** *IEEE MICRO*
  Chen, M. K., Olukotun, K.
  2003; 23 (6): 26-35

- **Using thread-level speculation to simplify manual parallelization** *9th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*
  Prabhu, M. K., Olukotun, K.
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- **Using Thread-Level Speculation to Simplify Manual Parallelization**
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- **The Jrpm system for dynamically parallelizing Java programs** *30TH ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, PROCEEDINGS*
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- **TEST: A tracer for extracting speculative threads** *CGO 2003: INTERNATIONAL SYMPOSIUM ON CODE GENERATION AND OPTIMIZATION*
  Chen, M., Olukotun, K.
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- **The Jrpm System for Dynamically Parallelizing Java Programs**
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- **Targeting dynamic compilation for embedded environments** *USENIX ASSOCIATION PROCEEDINGS OF THE 2ND JAVA(TM) VIRTUAL MACHINE RESEARCH AND TECHNOLOGY SYMPOSIUM*
  Chen, M., Olukotun, K.
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- **Efficient state representation for symbolic simulation** *39TH DESIGN AUTOMATION CONFERENCE, PROCEEDINGS 2002*
  Bertacco, V., Olukotun, K.
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- **High bandwidth on-chip cache design** *IEEE TRANSACTIONS ON COMPUTERS*
  Wilson, K. M., Olukotun, K.
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- **The Stanford Hydra CMP** *IEEE MICRO*
  Hammond, L., Hubbert, B. A., Siu, M., Prabhu, M. K., Chen, M., Olukotun, K.
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  Yamauchi, T., Hammond, L., Olukotun, O. A., Arimoto, K.
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- **REMARC: Reconfigurable multimedia array coprocessor** *IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS*
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- **The Stanford Hydra CMP** *IEEE MICRO Magazine, March-April 2000, and presented at Hot Chips*
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- **Improving the Performance of Speculatively Parallel Applications on the Hydra CMP**
  Olukotun, K., Hammond, L., Willey, M.
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- **Data speculation support for a chip multiprocessor** *ACM SIGPLAN NOTICES*
  Hammond, L., Willey, R., Olukotun, K.
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- **Considerations in the Design of Hydra: A Multiprocessor-on-a-Chip Microarchitecture** *Stanford University Computer Systems Lab Technical Report CSL-TR-98-749*
  Hammond, L., Olukotun, K.
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- **Digital system simulation: Methodologies and examples** *35th Design Automation Conference*
  Olukotun, K., Heinrich, M., Ofelt, D.
  ASSOC COMPUTING MACHINERY.1998: 658–663

- **Exploiting method-level parallelism in single-threaded Java programs** *International Conference on Parallel Architectures and Compilation Techniques*
  Chen, M. K., Olukotun, K.
  IEEE COMPUTER SOC.1998: 176–184

- **DCP: an algorithm for datapath/control partitioning of synthesizable RTL models** *International Conference on Computer Design: VLSI in Computers and Processors*
  Lam, V. J., OLUKOTUN, K. A.
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- **Exploiting Method-Level Parallelism in Single-Threaded Java Programs**
  Chen, M., Olukotun, K.
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- **Multilevel optimization of pipelined caches** *IEEE TRANSACTIONS ON COMPUTERS*
  Olukotun, K., Mudge, T. N., Brown, R. B.
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  NAYFEH, B. A., Olukotun, K.
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  1997

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  LEVITT, J., Olukotun, K.
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- **Designing high bandwidth on-chip caches** *24th Annual International Symposium on Computer Architecture*
  Wilson, K. M., Olukotun, K.
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- **A Single-Chip Multiprocessor** *IEEE Computer Special Issue on "Billion-Transistor Processors"*
  Hammond, L., Nayfeh, Basem, A., Olukotun, K.
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- **Software and Hardware for Exploiting Speculative Parallelism with a Multiprocessor** *Stanford University Computer Systems Lab Technical Report CSL-TR-97-715*
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  LEVITT, J., Olukotun, K.
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  NAYFEH, B. A., Olukotun, K., Singh, J. P.
  I E E E, COMPUTER SOC PRESS.1996: 74–84

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  Nayfeh, E. A., Hammond, L., Olukotun, K.

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- **Emulation and prototyping of digital systems** *NATO Advanced Study Institute on Hardware/Software Co-Design*
  HELAIHEL, R., Olukotun, K.
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- **Increasing cache port efficiency for dynamic superscalar microprocessors** *23rd Annual International Symposium on Computer Architecture*
  Wilson, K. M., Olukotun, K., Rosenblum, M.
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