Stanford

Robert Madison Radway

Ph.D. Student in Electrical Engineering, admitted Autumn 2018

Publications

PUBLICATIONS

- **Three-Dimensional Stacked Neural Network Accelerator Architectures for AR/VR Applications** *IEEE MICRO*
  Yang, L., Radway, R., Chen, Y., Wu, T., Liu, H., Ansari, E., Chandra, V., Mitra, S., Beigne, E.
  2022; 42 (6): 116-124

- **CHIMERA: A 0.92-TOPS, 2.2-TOPS/W Edge AI Accelerator With 2-MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Prabhu, K., Gural, A., Khan, Z. F., Radway, R. M., Giordano, M., Koul, K., Doshi, R., Kustin, J. W., Liu, T., Lopes, G. B., Turbiner, V., Khwa, W., Chih, et al
  2022

- **RADAR: A Fast and Energy-Efficient Programming Technique for Multiple Bits-Per-Cell RRAM Arrays** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Le, B. Q., Levy, A., Wu, T. F., Radway, R. M., Hsieh, E., Zheng, X., Nelson, M., Raina, P., Wong, H., Wong, S., Mitra, S.
  2021; 68 (9): 4397-4403

- **Illusion of large on-chip memory by networked computing chips for neural network inference** *NATURE ELECTRONICS*
  Radway, R. M., Bartolo, A., Jolly, P. C., Khan, Z. F., Le, B. Q., Tandon, P., Wu, T. F., Xin, Y., Vianello, E., Vivet, P., Nowak, E., Wong, H., Aly, et al
  2021

- **A 43pJ/Cycle Non-Volatile Microcontroller with 4.7 mu s Shutdown/Wake-up Integrating 2.3-bit/Cell Resistive RAM and Resilience Techniques**
  Wu, T. F., Le, B. Q., Radway, R., Bartolo, A., Hwang, W., Jeong, S., Li, H., Tandon, P., Vianello, E., Vivet, P., Nowak, E., Wootters, M. K., Wong, et al
  IEEE.2019: 226-+