Stanford

Priyanka Raina

Assistant Professor of Electrical Engineering and, by courtesy, of Computer Science

Curriculum Vitae available Online

CONTACT INFORMATION

- **Administrator**

  Julie Kline - EE Faculty Administrator

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  Tel (650) 723-4539

Bio

BIO

Priyanka Raina is an Assistant Professor in Electrical Engineering at Stanford University. Previously, she was a Visiting Research Scientist in the Architecture Research Group at NVIDIA Corporation. She received her Ph.D. degree in 2018 and S.M. degree in 2013 in Electrical Engineering and Computer Science from MIT and her B.Tech. degree in Electrical Engineering from Indian Institute of Technology (IIT) Delhi in 2011. Priyanka's current research interests are designing energy-efficient and high-performance circuits and systems for image, vision and machine learning applications on mobile devices, integrating emerging non volatile memory technologies in accelerator architectures, and creating frameworks for improving hardware/software system design productivity.

ACADEMIC APPOINTMENTS

- Assistant Professor, Electrical Engineering
- Assistant Professor (By courtesy), Computer Science

HONORS AND AWARDS

- Hellman Fellow, Stanford (2019)
- Best Young Scientist Paper Award, ESSCIRC 2016 (2017)
- ISSCC Student Research Preview Award, ISSCC 2016 (2017)
- Bimla Jain Medal, IIT Delhi (2011)
- Institute Silver Medal, IIT Delhi (2011)
- Gold Medal at Indian National Chemistry Olympiad, InChO (2007)

PROFESSIONAL EDUCATION

- Ph.D., Massachusetts Institute of Technology (MIT) , Electrical Engineering and Computer Science (2018)
- S.M., Massachusetts Institute of Technology (MIT) , Electrical Engineering and Computer Science (2013)
- B.Tech., Indian Institute of Technology (IIT) Delhi , Electrical Engineering (2011)

LINKS

- https://stanfordaccelerate.github.io: https://stanfordaccelerate.github.io

Research & Scholarship

CURRENT RESEARCH AND SCHOLARLY INTERESTS

For Priyanka's research please visit her group research page at https://stanfordaccelerate.github.io

Teaching

COURSES

2021-22

- Design Projects in VLSI Systems I: EE 272 (Win)
- Design Projects in VLSI Systems II: EE 372 (Spr)
- Emerging Non-Volatile Memory Devices and Circuit Design: EE 309B (Win)
- Introduction to VLSI Systems: EE 271 (Aut)
- Semiconductor Memory Devices and Circuit Design: EE 309A (Aut)

2020-21

- Design Projects in VLSI Systems I: EE 272A (Win)
- Design Projects in VLSI Systems II: EE 272B (Spr)
- Emerging Non-Volatile Memory Devices and Circuit Design: EE 309B (Win)
- Semiconductor Memory Devices and Circuit Design: EE 309A (Aut)

2019-20

- Design Projects in VLSI Systems: EE 272 (Win)
- Introduction to VLSI Systems: EE 271 (Aut)

2018-19

- Design Projects in VLSI Systems: EE 272 (Win)
- Introduction to VLSI Systems: EE 271 (Aut)

STANFORD ADVISEES

Doctoral Dissertation Reader (AC)

Nikhil Bhagdikar, Alex Carsello, Rohan Doshi, Massimo Giordano, Taeyoung Kong, Qiaoyi(Joey) Liu, Shuhan Liu, Zachary Myers, Ankita Nayak, Gedeon Nyengele, Alex Rucker, Kavya Sreedhar, Maxwell Strange, Tian Zhao

Doctoral Dissertation Advisor (AC)

Po-Han Chen, Kathleen Feng, Kalhan Koul, Akash Levy, Jackson Melchert

Master's Program Advisor

John Espera, Kavya Somasi, Jeffrey Yu

Doctoral (Program)

Po-Han Chen, Nikhil Poole, Kartik Prabhu, Khushal Sethi, Ritvik Sharma

Publications

PUBLICATIONS

- **CHIMERA: A 0.92-TOPS, 2.2-TOPS/W Edge AI Accelerator With 2-MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Prabhu, K., Gural, A., Khan, Z. F., Radway, R. M., Giordano, M., Koul, K., Doshi, R., Kustin, J. W., Liu, T., Lopes, G. B., Turbiner, V., Khwa, W., Chih, et al
  2022

- **Efficient Routing for Coarse-Grained Reconfigurable Arrays using Multi-Pole NEM Relays** *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*
  Levy, A., Oduoza, M., Balasingam, A., Howe, R., Raina, P.
  2022

- **Enabling Reusable Physical Design Flows with Modular Flow Generators** *Design Automation Conference (DAC)*
  Carsello, A., Thomas, J., Nayak, A., Chen, P., Horowitz, M., Raina, P., Torng, C.
  2022

- **An Agile Approach to the Design of Hardware Accelerators and Adaptable Compilers** *GOMACTech*
  Daly, R., Melchert, J., Koul, K., Raina, P., et al
  2022

- **SAPIENS: A 64-kb RRAM-Based Non-Volatile Associative Memory for One-Shot Learning and Inference at the Edge** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Li, H., Chen, W., Levy, A., Wang, C., Wang, H., Chen, P., Wan, W., Khwa, W., Chuang, H., Chih, Y., Chang, M., Wong, H., Raina, et al
  2021; 68 (12): 6637-6643

- **RADAR: A Fast and Energy-Efficient Programming Technique for Multiple Bits-Per-Cell RRAM Arrays** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Le, B. Q., Levy, A., Wu, T. F., Radway, R. M., Hsieh, E., Zheng, X., Nelson, M., Raina, P., Wong, H., Wong, S., Mitra, S.
  2021; 68 (9): 4397-4403

- **Simba: Scaling Deep-Learning Inference with Chiplet-Based Architecture** *COMMUNICATIONS OF THE ACM*
  Shao, Y., Cemons, J., Venkatesan, R., Zimmer, B., Fojtik, M., Jiang, N., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Tell, S. G., Zhang, Y., Dally, et al
  2021; 64 (6): 107-116

- **Best Papers From Hot Chips 32** *IEEE MICRO*
  Raina, P., Young, C.
  2021; 41 (2): 6

- **Automated Codesign of Domain-Specific Hardware Accelerators and Compilers**
  Raina, P., Kjolstad, F. B., Horowitz, M., Barrett, C., Fatahalian, K.
  ASCR Workshop on Reimagining Codesign.
  2021

- **CHIMERA: A 0.92 TOPS, 2.2 TOPS/W Edge AI Accelerator with 2 MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference** *Symposium on VLSI Circuits (VLSI)*
  Giordano, M., Prabhu, K., Koul, K., Radway, R. M., Gural, A., Doshi, R., Khan, Z. F., Kustin, J. W., Liu, T., Lopes, G. B., Turbiner, V., Khwa, W., Chih, et al
  2021

- **One-Shot Learning with Memory-Augmented Neural Networks Using a 64-kbit, 118 GOPS/W RRAM-Based Non-Volatile Associative Memory** *Symposium on VLSI Technology (VLSI)*
  Li, H., Chen, W., Levy, A., Wang, C., Wang, H., Chen, P., Wan, W., Wong, H., Raina, P.
  2021

- **A 0.32-128 TOPS, Scalable Multi-Chip-Module-Based Deep Neural Network Inference Accelerator With Ground-Referenced Signaling in 16 nm** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Zimmer, B., Venkatesan, R., Shao, Y., Clemons, J., Fojtik, M., Jiang, N., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Tell, S. G., Zhang, Y., Dally, et al
  2020; 55 (4): 920–32

- **Automating Vitiligo Skin Lesion Segmentation Using Convolutional Neural Networks**
  Low, M., Raina, P.
  IEEE International Symposium on Biomedical Imaging (ISBI).
  2020
- **A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing**
  Wan, W., Kubendran, R., Gao, B., Joshi, S., Raina, P., Wu, H., Cauwenberghs, G., Wong, H., IEEE
  IEEE.2020
- **Monte Carlo Simulation of a Three-Terminal RRAM with Applications to Neuromorphic Computing**
  Balasingam, A., Levy, A., Li, H., Raina, P., IEEE
  IEEE.2020: 197–99
- **Creating an Agile Hardware Design Flow**
  Bahr, R., Barrett, C., Bhagdikar, N., Carsello, A., Daly, R., Donovick, C., Durst, D., Fatahalian, K., Feng, K., Hanrahan, P., Hofstee, T., Horowitz, M., Huff, et al
  IEEE.2020
- **A-QED Verification of Hardware Accelerators**
  Singh, E., Lonsing, F., Chattopadhyay, S., Strange, M., Wei, P., Zhang, X., Zhou, Y., Chen, D., Cong, J., Raina, P., Zhang, Z., Barrett, C., Mitra, et al
  IEEE.2020
- **A 74TMACS/W CMOS-ReRAM Neurosynaptic Core with Dynamically Reconfigurable Dataflow and In-Situ Transposable Weights for Probabilistic Graphical Models**
  Wan, W., Kubendran, R., Eryilmaz, S., Zhang, W., Liao, Y., Wu, D., Deiss, S., Gao, B., Raina, P., Joshi, S., Wu, H., Cauwenberghs, G., Wong, et al
  International Solid-State Circuits Conference (ISSCC).
  2020
- **A Framework for Adding Low-Overhead, Fine-Grained Power Domains to CGRAs**
  Nayak, A., Zhang, K., Setaluri, R., Carsello, A., Mann, M., Richardson, S., Bahr, R., Hanrahan, P., Horowitz, M., Raina, P.
  Design, Automation and Test in Europe Conference (DATE).
  2020
- **Using Halide's Scheduling Language to Analyze DNN Accelerators**
  Yang, X., Gao, M., Liu, Q., Pu, J., Nayak, A., Setter, J., Bell, S., Cao, K., Ha, H., Raina, P., Kozyrakis, C., Horowitz, M.
  International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS).
  2020
- **A 0.11 pJ/Op, 0.32-128 TOPS, Scalable Multi-Chip-Module-based Deep Neural Network Accelerator with Ground-Reference Signaling in 16nm**
  Zimmer, B., Venkatesan, R., Shao, Y., Clemons, J., Fojtik, M., Jiang, N., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Tell, S. G., Zhang, Y., Dally, et al
  IEEE.2019: C300–C301
- **MAGNet: A Modular Accelerator Generator for Neural Networks**
  Venkatesan, R., Shao, Y., Wang, M., Clemons, J., Dai, S., Fojtik, M., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Zhang, Y., Zimmer, B., Dally, et al
  IEEE.2019
- **Neuro-inspired computing with emerging memories: where device physics meets learning algorithms**
  Li, H., Raina, P., Wong, H., Drouhin, H. J., Wegrowe, J. E., Razeghi, M., Jaffres, H.
  SPIE-INT SOC OPTICAL ENGINEERING.2019
- **A 0.11 pJ/Op, 0.32-128 TOPS, Scalable Multi-Chip-Module-based Deep Neural Network Accelerator Designed with a High-Productivity VLSI Methodology**
  Khailany, B., Venkatesan, R., Shao, Y., Zimmer, B., Clemons, J., Fojtik, M., Jiang, N., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Tell, S., Zhang, et al
  Hot Chips: A Symposium on High Performance Chips (HotChips).
  2019
- **Creating An Agile Hardware Flow**
  Bahr, R., Barrett, C., Bhagdikar, N., Carsello, A., Chizgi, N., Daly, R., Donovick, C., Durst, D., Fatahalian, K., Hanrahan, P., Hofstee, T., Horowitz, M., Huff, et al
  Hot Chips: A Symposium on High Performance Chips (HotChips).
  2019

- **Simba: Scaling Deep-Learning Inference with Multi-Chip-Module-Based Architecture**
  Shao, S., Clemons, J., Venkatesan, R., Zimmer, B., Fojtik, M., Jiang, N., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Tell, S., Zhang, Y., Dally, et al
  International Symposium on Microarchitecture (MICRO).
  2019
- **Timeloop: A Systematic Approach to DNN Accelerator Evaluation**
  Parashar, A., Raina, P., Shao, Y., Chen, Y., Ying, V. A., Mukkara, A., Venkatesan, R., Khailany, B., Keckler, S. W., Emer, J., IEEE
  IEEE.2019: 304–15
- **An Energy-Scalable Accelerator for Blind Image Deblurring**
  Raina, P., Tikekar, M., Chandrakasan, A. P.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2017: 1849–62
- **A 0.6V 8mW 3D Vision Processor for a Navigation Device for the Visually Impaired**
  Jeon, D., Ickes, N., Raina, P., Wang, H., Rus, D., Chandrakasan, A., IEEE
  IEEE.2016: 416–U584
- **An Energy-Scalable Accelerator for Blind Image Deblurring**
  Raina, P., Tikekar, M., Chandrakasan, A. P., IEEE
  IEEE.2016: 113–16
- **Reconfigurable Processor for Energy-Efficient Computational Photography**
  Rithe, R., Raina, P., Ickes, N., Tenneti, S. V., Chandrakasan, A. P.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2013: 2908–19
- **Reconfigurable Processor for Energy-Scalable Computational Photography**
  Rithe, R., Raina, P., Ickes, N., Tenneti, S. V., Chandrakasan, A. P., IEEE
  IEEE.2013: 164–U972

PRESENTATIONS

- Low-Power Processor for Real-Time Motion Magnification in Videos - Microsystems Annual Research Conference
- Circuits & Systems for Computational Imaging on Mobile Devices - Rising Stars Workshop
- Energy-Scalable Accelerator for Blind Image Deblurring - ESSCIRC
- Energy-Scalable Accelerator for Blind Image Deblurring - ISSCC Student Research Preview
- Energy-Scalable Accelerator for Blind Image Deblurring - Microsystems Annual Research Conference