Stanford

Priyanka Raina

Associate Professor of Electrical Engineering and, by courtesy, of Computer Science

Curriculum Vitae available Online

CONTACT INFORMATION

- **Administrator**

  Julie Kline - EE Faculty Administrator

  Email klinej@stanford.edu

  Tel (650) 723-4539

Bio

BIO

Priyanka Raina received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Delhi, New Delhi, India, in 2011, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2013 and 2018, respectively. She was a Visiting Research Scientist with NVIDIA Corporation, Santa Clara, CA, USA, in 2018. She is currently an Associate Professor of electrical engineering with Stanford University, Stanford, CA, USA, where she works on domain-specific hardware architectures and agile hardware–software codesign methodology.

Dr. Raina is a 2018 Terman Faculty Fellow. She was a co-recipient of the Best Demo Paper Award at VLSI 2022, the Best Student Paper Award at VLSI 2021, the IEEE Journal of Solid-State Circuits (JSSC) Best Paper Award in 2020, the Best Paper Award at MICRO 2019, and the Best Young Scientist Paper Award at ESSCIRC 2016. She has won the DARPA Young Faculty Award in 2024, Sloan Research Fellowship in 2024, the National Science Foundation (NSF) CAREER Award in 2023, the Intel Rising Star Faculty Award in 2021, and the Hellman Faculty Scholar Award in 2019. She was the Program Chair of the IEEE Hot Chips in 2020. She serves as an Associate Editor for the IEEE Journal of Solid-State Circuits and IEEE Solid-State Circuits Letters.

ACADEMIC APPOINTMENTS

- Associate Professor, Electrical Engineering
- Associate Professor (By courtesy), Computer Science

HONORS AND AWARDS

- DARPA Young Faculty Award, Stanford University (2024)
- Sloan Research Fellowship, Stanford University (2024)
- NSF CAREER Award, Stanford University (2023)
- ISSCC Student Research Preview Award, Stanford University (2022)
- VLSI Best Demo Paper Award, Stanford University (2022)
- Intel Rising Star Faculty Award, Stanford University (2021)

- VLSI Best Student Paper Award, Stanford University (2021)
- JSSC Best Paper Award, Stanford University (2020)
- Hellman Fellow, Stanford University (2019)
- MICRO Best Paper Award, Stanford University (2019)
- Terman Faculty Fellow, Stanford University (2018)
- Terman Faculty Fellow, MIT (2017)
- ESSCIRC Best Young Scientist Paper Award, MIT (2016)
- ISSCC Student Research Preview Award, MIT (2016)
- Bimla Jain Medal, IIT Delhi (2011)
- Institute Silver Medal, IIT Delhi (2011)
- Gold Medal at Indian National Chemistry Olympiad, InChO (2007)

PROGRAM AFFILIATIONS

- Stanford SystemX Alliance

PROFESSIONAL EDUCATION

- Ph.D., Massachusetts Institute of Technology (MIT) , Electrical Engineering and Computer Science (2018)
- S.M., Massachusetts Institute of Technology (MIT) , Electrical Engineering and Computer Science (2013)
- B.Tech., Indian Institute of Technology (IIT) Delhi , Electrical Engineering (2011)

LINKS

- https://stanfordaccelerate.github.io: https://stanfordaccelerate.github.io
- https://priyanka-raina.github.io/: https://priyanka-raina.github.io/

Research & Scholarship

CURRENT RESEARCH AND SCHOLARLY INTERESTS

For Priyanka's research please visit her group research page at https://stanfordaccelerate.github.io

Teaching

COURSES

2026-27

- Design Projects in VLSI Systems I: EE 272 (Win)
- Design Projects in VLSI Systems II: EE 372 (Spr)
- Efficient ML Infrastructure at Scale: CS 349E, EE 339 (Aut)

2025-26

- Semiconductor Memory Devices and Circuit Design: EE 309A (Aut)

2024-25

- Design Projects in VLSI Systems I: EE 272 (Win)
- Design Projects in VLSI Systems II: EE 372 (Spr)

2023-24

- Design Projects in VLSI Systems I: EE 272 (Win)

- Emerging Non-Volatile Memory Devices and Circuit Design: EE 309B (Win)
- Semiconductor Memory Devices and Circuit Design: EE 309A (Aut)

STANFORD ADVISEES

Doctoral Dissertation Reader (AC)

Maxwell Strange, Can WANG

Orals Chair

Scott Kovach, Haoran Xu

Doctoral Dissertation Advisor (AC)

Po-Han Chen, Bo Wun Cheng, Yuchen Mei, Michael Oduoza, Allen Pan, Zhouhua Xie, Jeffrey Yu

Master's Program Advisor

Bucky Aboud-Hall, Javed Chowdhury, Jack Griffin, Abdalazeez Jerby, Jaeyoung Kil, Daniel Rullan, Eddie Rydell, Neo Vasudeva, Suze van Adrichem

Doctoral (Program)

Po-Han Chen, Bo Wun Cheng, Evan Lai, Yuchen Mei, Michael Oduoza, Allen Pan, Nikhil Poole, Sai Gautham Ravipati, Ritvik Sharma, Jan Strzeszynski, Jeffrey Yu

Publications

PUBLICATIONS

- **A methodology for accurate benchmarking of neural network accelerators using a high-level synthesis-based hardware generator.** *Philosophical transactions. Series A, Mathematical, physical, and engineering sciences*
  Prabhu, K., Yu, J., Pan, X. A., Raina, P.
  2026; 384 (2315)
- **Onyx: A 12-nm Programmable Accelerator for Dense and Sparse Applications** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Koul, K., Hsu, O., Mei, Y., Ravipati, S., Strange, M., Melchert, J., Carsello, A., Kong, T., Chen, P., Ke, H., Zhang, K., Liu, Q., Nyengele, et al
  2025
- **Designing Programmable Accelerators for Sparse Tensor Algebra** *IEEE MICRO*
  Koul, K., Xie, Z., Strange, M., Ravipati, S., Cheng, B., Hsu, O., Chen, P., Horowitz, M., Kjolstad, F., Raina, P.
  2025; 45 (3): 58-65
- **Monolithic 3-D Integration of Diverse Memories: Resistive Switching (RRAM) and Gain Cell (GC) Memory Integrated on Si CMOS** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Liu, S., Radway, R. M., Wang, X., Moro, F., Nodin, J., Jana, K., Yan, L., Du, S., Upton, L. R., Chen, W., Kang, J., Chen, J., Li, et al
  2025
- **MINOTAUR: A Posit-Based 0.42-0.50-TOPS/W Edge Transformer Inference and Training Accelerator** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Prabhu, K., Radway, R. M., Yu, J., Bartolone, K., Giordano, M., Peddinghaus, F., Urman, Y., Khwa, W., Chih, Y., Chang, M., Mitra, S., Raina, P.
  2025; 60 (4): 1311-1323
- **Automated Translation Validation of a Compiler for Statically Scheduled Accelerators** *Formal Methods in Computer-Aided Design (FMCAD)*
  Melchert, J., et al
  2025
- **Aspen: A 630 FPS Real-Time Posit-Based Unified Accelerator for Extended Reality Perception Workloads** *IEEE Custom Integrated Circuits Conference (CICC)*
  Feng, K., et al
  2025

- **Opal: A 16nm Coarse-Grained Reconfigurable Array for Full Sparse ML Applications** *IEEE Custom Integrated Circuits Conference (CICC)*
  Chen, P., et al
  2025
- **Birch: A Real-Time Accelerator for Multi-Task Mixed-Domain Extended Reality Perception Workloads** *IEEE Asian Solid-State Circuits Conference (A-SSCC)*
  Feng, K., et al
  2025
- **Opal: A 16-nm Coarse-Grained Reconfigurable Array SoC for Full Sparse Machine Learning Applications** *IEEE SOLID-STATE CIRCUITS LETTERS*
  Chen, P., Wun Cheng, B., Oduoza, M., Xie, Z., Lu, R., Gautham Ravipati, S., Koul, K., Carsello, A., Mei, Y., Horowitz, M., Raina, P.
  2025; 8: 293-296
- **Cascade: An Application Pipelining Toolkit for Coarse-Grained Reconfigurable Arrays** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Melchert, J., Mei, Y., Koul, K., Liu, Q., Horowitz, M., Raina, P.
  2024; 43 (10): 3055-3067
- **EMBER: Efficient Multiple-Bits-Per-Cell Embedded RRAM Macro for High-Density Digital Storage** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Levy, A., Upton, L. R., Scott, M. D., Rich, D., Khwa, W., Chih, Y., Chang, M., Mitra, S., Murmann, B., Raina, P.
  2024
- **Cascade: An Application Pipelining Toolkit for Coarse-Grained Reconfigurable Arrays**
  Melchert, J., et al
  Languages, Tools, and Techniques for Accelerator Design (LATTE) Workshop at the ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS).
  2024
- **AHA: An Open-Source Framework for Co-design of Programmable Accelerators and Compilers** *Open-Source Computer Architecture Research (OSCAR) Workshop at the International Symposium on Computer Architecture (ISCA)*
  Koul, K., et al
  2024
- **PEak: A Single Source of Truth for Hardware Design and Verification** *ACM Transactions on Embedded Computing Systems (TECS)*
  Donovick, C., et al
  2024
- **8-bit Transformer Inference and Fine-tuning for Edge Accelerators**
  Yu, J., Prabhu, K., Urman, Y., Radway, R. M., Han, E., Raina, P., ACM
  ASSOC COMPUTING MACHINERY.2024: 5-21
- **A High-Level Synthesis Based Framework for Design Space Exploration and Generation of Neural Network Accelerators** *AI for Fully-Automated Chip Design (AI4FACD) Workshop at the International Symposium on Computer Architecture (ISCA)*
  Prabhu, K., et al
  2024
- **Onyx: A Programmable Accelerator for Sparse Tensor Algebra** *IEEE Hot Chips Symposium (Hot Chips)*
  Koul, K., et al
  2024
- **Efficiently Synthesizing Lowest Cost Rewrite Rules for Instruction Selection** *Formal Methods in Computer-Aided Design (FMCAD)*
  Daly, R., et al
  2024
- **Edge Continual Training and Inference with RRAM-Gain Cell Memory Integrated on Si CMOS** *IEEE International Electron Devices Meeting (IEDM)*
  Liu, S., et al
  2024

- **FastPASE: An AI-Driven Fast PPA Speculation Engine for RTL Design Space Optimization**
  Levy, A., Walston, J., Samanta, S., Raina, P., Diamantidis, S., IEEE
  IEEE.2024

- **MINOTAUR: An Edge Transformer Inference and Training Accelerator with 12 MBytes On-Chip Resistive RAM and Fine-Grained Spatiotemporal Power Gating** *IEEE Symposium on VLSI Technology & Circuits (VLSI)*
  Prabhu, K., et al
  2024

- **Onyx: A 12nm 756 GOPS/W Coarse-Grained Reconfigurable Array for Accelerating Dense and Sparse Applications** *IEEE Symposium on VLSI Technology & Circuits (VLSI)*
  Koul, K., Strange, M., Melchert, J., Carsello, A., Mei, Y., Hsu, O., Kong, T., Chen, P., Ke, H., Zhang, K., Liu, Q., Nyengele, G., Balasingam, et al
  2024: 1-2

- **Amber: A 16-nm System-on-Chip With a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Feng, K., Kong, T., Koul, K., Melchert, J., Carsello, A., Liu, Q., Nyengele, G., Strange, M., Zhang, K., Nayak, A., Setter, J., Thomas, J., Sreedhar, et al
  2023

- **3-D coarse-grained reconfigurable array using multi-pole NEM relays for programmable routing** *INTEGRATION-THE VLSI JOURNAL*
  Levy, A., Oduoza, M., Balasingam, A., Howe, R. T., Raina, P.
  2023; 88: 249-261

- **APEX: A Framework for Automated Processing Element Design Space Exploration using Frequent Subgraph Analysis** *ASPLOS 2023: Proceedings of the 28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems*
  Melchert, J., Feng, K., Donovick, C., Daly, R., Sharma, R., Barrett, C., Horowitz, M., Hanrahan, P., Raina, P.
  2023

- **Canal: A Flexible Interconnect Generator for Coarse-Grained Reconfigurable Arrays** *IEEE Computer Architecture Letters*
  Melchert, J., Zhang, K., Mei, Y., Horowitz, M., Torng, C., Raina, P.
  2023

- **Ultra-Dense 3D Physical Design Unlocks New Architectural Design Points with Large Benefits**
  Srimani, T., Radway, R. M., Kim, J., Prabhu, K., Rich, D., Gilardi, C., Raina, P., Shulaker, M., Lim, S., Mitra, S.
  edited by IEEE
  IEEE.2023

- **Unified Buffer: Compiling Image Processing and Machine Learning Applications to Push-Memory Accelerators** *ACM Transactions on Architecture and Code Optimization*
  Liu, Q., Setter, J., Huff, D., Strange, M., Feng, K., Horowitz, M., Raina, P., Kjolstad, F.
  2023: 26

- **An Open-Source 4x8 Coarse-Grained Reconfigurable Array Using SkyWater 130 nm Technology and Agile Hardware Design Flow**
  Chen, P., Tsao, C., Raina, P., IEEE
  IEEE.2023

- **EMBER: A 100 MHz, 0.86 mm², Multiple-Bits-per-Cell RRAM Macro in 40 nm CMOS with Compact Peripherals and 1.0 pJ/bit Read Circuitry**
  Upton, L. R., Levy, A., Scott, M. D., Rich, D., Khwa, W., Chih, Y., Chang, M., Mitra, S., Raina, P., Murmann, B., IEEE
  IEEE.2023: 469-472

- **AHA: An Agile Approach to the Design of Coarse-Grained Reconfigurable Accelerators and Compilers** *ACM Transactions on Embedded Computing Systems*
  Koul, K., Melchert, J., Sreedhar, K., Truong, L., Nyengele, G., Zhang, K., Liu, Q., Setter, J., Chen, P., Mei, Y., Strange, M., Daly, R., Donovick, et al
  2023; 22 (2)

- **PEak: A Single Source of Truth for Hardware Design and Verification**
  Donovick, C., et al
  Programming Languages for Architecture (PLARCH) Workshop at PLDI.
  2023

- **APEX: A Framework for Automated Processing Element Design Space Exploration using Frequent Subgraph Analysis** *ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*
  Melchert, J., et al
  2023

- **PBA: Percentile-Based Level Allocation for Multiple-Bits-Per-Cell RRAM**
  Wei, A., Levy, A., Yi, P., Radway, R. M., Raina, P., Mitra, S., Achour, S., IEEE
  IEEE.2023

- **High-density analog image storage in an analog-valued non-volatile memory array** *NEUROMORPHIC COMPUTING AND ENGINEERING*
  Zheng, X., Zarcone, R., Levy, A., Khwa, W., Raina, P., Olshausen, B. A., Wong, H.
  2022; 2 (4)

- **A compute-in-memory chip based on resistive random-access memory.** *Nature*
  Wan, W., Kubendran, R., Schaefer, C., Eryilmaz, S. B., Zhang, W., Wu, D., Deiss, S., Raina, P., Qian, H., Gao, B., Joshi, S., Wu, H., Wong, et al
  2022; 608 (7923): 504-512

- **CHIMERA: A 0.92-TOPS, 2.2-TOPS/W Edge AI Accelerator With 2-MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Prabhu, K., Gural, A., Khan, Z. F., Radway, R. M., Giordano, M., Koul, K., Doshi, R., Kustin, J. W., Liu, T., Lopes, G. B., Turbiner, V., Khwa, W., Chih, et al
  2022

- **Efficient Routing for Coarse-Grained Reconfigurable Arrays using Multi-Pole NEM Relays** *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*
  Levy, A., Oduoza, M., Balasingam, A., Howe, R., Raina, P.
  2022

- **mflowgen: a modular flow generator and ecosystem for community-driven physical design** *DAC '22: Proceedings of the 59th ACM/IEEE Design Automation Conference*
  Carsello, A., Thomas, J., Nayak, A., Chen, P., Horowitz, M., Raina, P., Torng, C.
  2022: 1339–1342

- **Synthesizing Instruction Selection Rewrite Rules from RTL using SMT**
  Daly, R., Donovick, C., Melchert, J., Setaluri, R., Bullock, N., Raina, P., Barrett, C., Hanrahan, P.
  edited by Griggio, A., Rungta, N.
  TU Wien Acad Press.2022: 139-150

- **Improving Energy Efficiency of CGRAs with Low-Overhead Fine-Grained Power Domains** *ACM Transactions on Reconfigurable Technology and Systems*
  Nayak, A., Zhang, K., Setaluri, R., Carsello, A., Mann, M., Torng, C., Richardson, S., Bahr, R., Hanrahan, P., Horowitz, M., Raina, P.
  2022

- **Canal: A Flexible Interconnect Generator for Coarse-Grained Reconfigurable Arrays**
  Melchert, J., et al
  Workshop on Democratizing Domain-Specific Accelerators (WDDSA) at MICRO.
  2022

- **Hardware Abstractions and Hardware Mechanisms to Support Multi-Task Execution on Coarse-Grained Reconfigurable Arrays**
  Kong, T., et al
  Workshop on Democratizing Domain-Specific Accelerators (WDDSA) at MICRO.
  2022

- **Amber: Coarse-Grained Reconfigurable Array-Based SoC for Dense Linear Algebra Acceleration** *IEEE Hot Chips Symposium (Hot Chips)*
  Feng, K., et al
  2022

- **Amber: A 367 GOPS, 538 GOPS/W 16nm SoC with a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra** *IEEE Symposium on VLSI Technology & Circuits (VLSI)*
  Carsello, A., et al

2022

- **An Agile Approach to the Design of Hardware Accelerators and Adaptable Compilers** *GOMACTech*
  Daly, R., Melchert, J., Koul, K., Raina, P., et al
  2022

- **SAPIENS: A 64-kb RRAM-Based Non-Volatile Associative Memory for One-Shot Learning and Inference at the Edge** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Li, H., Chen, W., Levy, A., Wang, C., Wang, H., Chen, P., Wan, W., Khwa, W., Chuang, H., Chih, Y., Chang, M., Wong, H., Raina, et al
  2021; 68 (12): 6637-6643

- **RADAR: A Fast and Energy-Efficient Programming Technique for Multiple Bits-Per-Cell RRAM Arrays** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Le, B. Q., Levy, A., Wu, T. F., Radway, R. M., Hsieh, E., Zheng, X., Nelson, M., Raina, P., Wong, H., Wong, S., Mitra, S.
  2021; 68 (9): 4397-4403

- **Simba: Scaling Deep-Learning Inference with Chiplet-Based Architecture** *COMMUNICATIONS OF THE ACM*
  Shao, Y., Cemons, J., Venkatesan, R., Zimmer, B., Fojtik, M., Jiang, N., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Tell, S. G., Zhang, Y., Dally, et al
  2021; 64 (6): 107-116

- **Automated Codesign of Domain-Specific Hardware Accelerators and Compilers**
  Raina, P., Kjolstad, F. B., Horowitz, M., Barrett, C., Fatahalian, K.
  ASCR Workshop on Reimagining Codesign.
  2021

- **CHIMERA: A 0.92 TOPS, 2.2 TOPS/W Edge AI Accelerator with 2 MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference** *Symposium on VLSI Circuits (VLSI)*
  Giordano, M., Prabhu, K., Koul, K., Radway, R. M., Gural, A., Doshi, R., Khan, Z. F., Kustin, J. W., Liu, T., Lopes, G. B., Turbiner, V., Khwa, W., Chih, et al
  2021

- **One-Shot Learning with Memory-Augmented Neural Networks Using a 64-kbit, 118 GOPS/W RRAM-Based Non-Volatile Associative Memory** *Symposium on VLSI Technology (VLSI)*
  Li, H., Chen, W., Levy, A., Wang, C., Wang, H., Chen, P., Wan, W., Wong, H., Raina, P.
  2021

- **A 0.32-128 TOPS, Scalable Multi-Chip-Module-Based Deep Neural Network Inference Accelerator With Ground-Referenced Signaling in 16 nm** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Zimmer, B., Venkatesan, R., Shao, Y., Clemons, J., Fojtik, M., Jiang, N., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Tell, S. G., Zhang, Y., Dally, et al
  2020; 55 (4): 920–32

- **Automating Vitiligo Skin Lesion Segmentation Using Convolutional Neural Networks**
  Low, M., Raina, P.
  IEEE International Symposium on Biomedical Imaging (ISBI).
  2020

- **A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing**
  Wan, W., Kubendran, R., Gao, B., Joshi, S., Raina, P., Wu, H., Cauwenberghs, G., Wong, H., IEEE
  IEEE.2020

- **Monte Carlo Simulation of a Three-Terminal RRAM with Applications to Neuromorphic Computing**
  Balasingam, A., Levy, A., Li, H., Raina, P., IEEE
  IEEE.2020: 197–99

- **Creating an Agile Hardware Design Flow**
  Bahr, R., Barrett, C., Bhagdikar, N., Carsello, A., Daly, R., Donovick, C., Durst, D., Fatahalian, K., Feng, K., Hanrahan, P., Hofstee, T., Horowitz, M., Huff, et al
  IEEE.2020

- **A-QED Verification of Hardware Accelerators**
  Singh, E., Lonsing, F., Chattopadhyay, S., Strange, M., Wei, P., Zhang, X., Zhou, Y., Chen, D., Cong, J., Raina, P., Zhang, Z., Barrett, C., Mitra, et al
  IEEE.2020

- **A 74TMACS/W CMOS-ReRAM Neurosynaptic Core with Dynamically Reconfigurable Dataflow and In-Situ Transposable Weights for Probabilistic Graphical Models**
  Wan, W., Kubendran, R., Eryilmaz, S., Zhang, W., Liao, Y., Wu, D., Deiss, S., Gao, B., Raina, P., Joshi, S., Wu, H., Cauwenberghs, G., Wong, et al
  International Solid-State Circuits Conference (ISSCC).
  2020

- **A Framework for Adding Low-Overhead, Fine-Grained Power Domains to CGRAs**
  Nayak, A., Zhang, K., Setaluri, R., Carsello, A., Mann, M., Richardson, S., Bahr, R., Hanrahan, P., Horowitz, M., Raina, P.
  Design, Automation and Test in Europe Conference (DATE).
  2020

- **Using Halide's Scheduling Language to Analyze DNN Accelerators**
  Yang, X., Gao, M., Liu, Q., Pu, J., Nayak, A., Setter, J., Bell, S., Cao, K., Ha, H., Raina, P., Kozyrakis, C., Horowitz, M.
  International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS).
  2020

- **A 0.11 pJ/Op, 0.32-128 TOPS, Scalable Multi-Chip-Module-based Deep Neural Network Accelerator with Ground-Reference Signaling in 16nm**
  Zimmer, B., Venkatesan, R., Shao, Y., Clemons, J., Fojtik, M., Jiang, N., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Tell, S. G., Zhang, Y., Dally, et al
  IEEE.2019: C300–C301

- **MAGNet: A Modular Accelerator Generator for Neural Networks**
  Venkatesan, R., Shao, Y., Wang, M., Clemons, J., Dai, S., Fojtik, M., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Zhang, Y., Zimmer, B., Dally, et al
  IEEE.2019

- **Neuro-inspired computing with emerging memories: where device physics meets learning algorithms**
  Li, H., Raina, P., Wong, H.
  edited by Drouhin, H. J., Wegrowe, J. E., Razeghi, M., Jaffres, H.
  SPIE-INT SOC OPTICAL ENGINEERING.2019

- **A 0.11 pJ/Op, 0.32-128 TOPS, Scalable Multi-Chip-Module-based Deep Neural Network Accelerator Designed with a High-Productivity VLSI Methodology**
  Khailany, B., Venkatesan, R., Shao, Y., Zimmer, B., Clemons, J., Fojtik, M., Jiang, N., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Tell, S., Zhang, et al
  Hot Chips: A Symposium on High Performance Chips (HotChips).
  2019

- **Creating An Agile Hardware Flow**
  Bahr, R., Barrett, C., Bhagdikar, N., Carsello, A., Chizgi, N., Daly, R., Donovick, C., Durst, D., Fatahalian, K., Hanrahan, P., Hofstee, T., Horowitz, M., Huff, et al
  Hot Chips: A Symposium on High Performance Chips (HotChips).
  2019

- **Simba: Scaling Deep-Learning Inference with Multi-Chip-Module-Based Architecture**
  Shao, S., Clemons, J., Venkatesan, R., Zimmer, B., Fojtik, M., Jiang, N., Keller, B., Klinefelter, A., Pinckney, N., Raina, P., Tell, S., Zhang, Y., Dally, et al
  International Symposium on Microarchitecture (MICRO).
  2019

- **Timeloop: A Systematic Approach to DNN Accelerator Evaluation**
  Parashar, A., Raina, P., Shao, Y., Chen, Y., Ying, V. A., Mukkara, A., Venkatesan, R., Khailany, B., Keckler, S. W., Emer, J., IEEE
  IEEE.2019: 304–15

- **An Energy-Scalable Accelerator for Blind Image Deblurring**

Raina, P., Tikekar, M., Chandrakasan, A. P.
IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2017: 1849–62

- **A 0.6V 8mW 3D Vision Processor for a Navigation Device for the Visually Impaired**
  Jeon, D., Ickes, N., Raina, P., Wang, H., Rus, D., Chandrakasan, A., IEEE
  IEEE.2016: 416–U584
- **An Energy-Scalable Accelerator for Blind Image Deblurring**
  Raina, P., Tikekar, M., Chandrakasan, A. P., IEEE
  IEEE.2016: 113–16
- **Reconfigurable Processor for Energy-Efficient Computational Photography**
  Rithe, R., Raina, P., Ickes, N., Tenneti, S. V., Chandrakasan, A. P.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2013: 2908–19
- **Reconfigurable Processor for Energy-Scalable Computational Photography**
  Rithe, R., Raina, P., Ickes, N., Tenneti, S. V., Chandrakasan, A. P., IEEE
  IEEE.2013: 164–U972