Stanford

Alex Carsello

Ph.D. Student in Electrical Engineering, admitted Autumn 2017

Bio

BIO

Alex is currently a Ph.D. student in Electrical Engineering advised by Mark Horowitz and affiliated with the AHA! Agile Hardware Center. He is interested in reconfigurable computing, domain-specific architectures for image processing, and hardware design methodology. He is currently working within the AHA Agile Hardware Project on a next-generation CGRA (coarse-grained reconfigurable architecture) chip generator. Alex received a B.S. in Electrical and Computer Engineering from Washington University in St. Louis in 2017.

EDUCATION AND CERTIFICATIONS

- M.S., Stanford University , Electrical Engineering (2020)
- B.S., Washington University in St. Louis , Electrical Engineering (2017)
- B.S., Washington University in St. Louis , Computer Engineering (2017)

Publications

PUBLICATIONS

- **Amber: A 16-nm System-on-Chip With a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Feng, K., Kong, T., Koul, K., Melchert, J., Carsello, A., Liu, Q., Nyengele, G., Strange, M., Zhang, K., Nayak, A., Setter, J., Thomas, J., Sreedhar, et al
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- **AHA: An Agile Approach to the Design of Coarse-Grained Reconfigurable Accelerators and Compilers** *ACM Transactions on Embedded Computing Systems*
  Koul, K., Melchert, J., Sreedhar, K., Truong, L., Nyengele, G., Zhang, K., Liu, Q., Setter, J., Chen, P., Mei, Y., Strange, M., Daly, R., Donovick, et al
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- **mflowgen: a modular flow generator and ecosystem for community-driven physical design** *DAC '22: Proceedings of the 59th ACM/IEEE Design Automation Conference*
  Carsello, A., Thomas, J., Nayak, A., Chen, P., Horowitz, M., Raina, P., Torng, C.
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- **Improving Energy Efficiency of CGRAs with Low-Overhead Fine-Grained Power Domains** *ACM Transactions on Reconfigurable Technology and Systems*
  Nayak, A., Zhang, K., Setaluri, R., Carsello, A., Mann, M., Torng, C., Richardson, S., Bahr, R., Hanrahan, P., Horowitz, M., Raina, P.
  2022
- **Amber: A 367 GOPS, 538 GOPS/W 16nm SoC with a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra** *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*
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- **A Framework for Adding Low-Overhead, Fine-Grained Power Domains to CGRAs**

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- **Creating an Agile Hardware Design Flow**

  Bahr, R., Barrett, C., Bhagdikar, N., Carsello, A., Daly, R., Donovick, C., Durst, D., Fatahalian, K., Feng, K., Hanrahan, P., Hofstee, T., Horowitz, M., Huff, et al

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