Stanford

Mark Horowitz

Yahoo! Founders Professor in the School of Engineering and Professor of Computer Science

Electrical Engineering

CONTACT INFORMATION

- **Administrative**

  Eiko Rutherford - Program Manager

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Bio

BIO

Professor Horowitz initially focused on designing high-performance digital systems by combining work in computer-aided design tools, circuit design, and system architecture. During this time, he built a number of early RISC microprocessors, and contributed to the design of early distributed shared memory multiprocessors. In 1990, Dr. Horowitz took leave from Stanford to help start Rambus Inc., a company designing high-bandwidth memory interface technology. After returning in 1991, his research group pioneered many innovations in high-speed link design, and many of today’s high speed link designs are designed by his former students or colleagues from Rambus.

In the 2000s he started a long collaboration with Prof. Levoy on computational photography, which included work that led to the Lytro camera, whose photographs could be refocused after they were captured.. Dr. Horowitz's current research interests are quite broad and span using EE and CS analysis methods to problems in neuro and molecular biology to creating new agile design methodologies for analog and digital VLSI circuits. He remains interested in learning new things, and building interdisciplinary teams.

ACADEMIC APPOINTMENTS

- Professor, Electrical Engineering
- Professor, Computer Science
- Member, Bio-X
- Affiliate, Precourt Institute for Energy
- Member, Wu Tsai Neurosciences Institute

HONORS AND AWARDS

- Eckert-Mauchly Award, ACM and IEEE Computer Society (2022)
- Faculty Researcher Award, SIA (2010)
- Donald O. Pederson Technical Field Award, IEEE (2006)
- Best Paper Award, ISQED (2005)

- Jack Kilby Outstanding Paper Award, ISSCC (2003)
- Most influential paper, International Symposium of Computer Arch (1994)
- Most Influential Paper, International Symposium on Computer Architecture (1989)
- Elected Fellow, Association for Computing Machinery
- Elected Fellow, IEEE

BOARDS, ADVISORY COMMITTEES, PROFESSIONAL ORGANIZATIONS

- Member, National Academy of Engineering (2013 - present)
- Member, Computer Science and Telecommunications Advisory Board, NAS (2013 - 2019)
- Member, American Academy of Arts and Sciences (2013 - present)

PROGRAM AFFILIATIONS

- Stanford SystemX Alliance

PROFESSIONAL EDUCATION

- PhD, Stanford University (1984)
- MS, MIT (1978)
- BS, MIT (1978)

PATENTS

- Gary B. Bronner, Brent S. Haukness, Mark A. Horowitz, Mark D. Kellam, Fariborz Assaderaghi. "United States Patent 11,244,727 Dynamic memory rank configuration", Rambus Inc, Feb 8, 2022
- Vladimir M Stojanovic, Andrew C Ho, Anthony Bessios, Bruno W Garlepp, Grace Tsang, Mark A Horowitz, Jared L Zerbe, Jason C Wei. "United States Patent 16/999,853 Partial response receiver", Rambus Inc, Mar 11, 2021
- Craig Hampel, Mark Horowitz. "United States Patent 17/000,130 System including hierarchical memory modules having different types of integrated circuit memory devices", Rambus Inc, Feb 4, 2021
- Mark Alan Horowitz, Ilias Pappas, Edward Buckley, William Thomas Blank. "United States Patent 10,861,380 Display systems with hybrid emitter circuits", Facebook Technologies LLC, Dec 8, 2020
- Haw-Jyh Liaw, Xingchao Yuan, Mark A Horowitz. "United States Patent 10,782,344 Technique for determining performance characteristics of electronic devices and systems", Rambus Inc, Sep 22, 2020
- Vladimir M Stojanovic, Andrew C Ho, Anthony Bessios, Fred F Chen, Elad Alon, Mark A Horowitz. "United States Patent 10,771,295 High speed signaling system with adaptive transmit pre-emphasis", Rambus Inc, Sep 8, 2020
- Vladimir M Stojanovic, Andrew C Ho, Anthony Bessios, Bruno W Garlepp, Grace Tsang, Mark A Horowitz, Jared L Zerbe, Jason C Wei. "United States Patent 10,764,094 Partial response receiver", Rambus Inc, Sep 1, 2020
- Craig Hampel, Mark Horowitz. "United States Patent 10,755,794 System including hierarchical memory modules having different types of integrated circuit memory devices", Rambus Inc, Aug 25, 2020
- Ely K Tsern, Mark A Horowitz, Frederick A Ware. "United States Patent 16/805,619 Memory Controller With Error Detection And Retry Modes Of Operation", Rambus Inc, Aug 20, 2020
- Ely K Tsern, Mark A Horowitz, Frederick A Ware. "United States Patent 10,621,023 Memory controller with error detection and retry modes of operation", Rambus Inc, Apr 14, 2020
- Vladimir M Stojanovic, Andrew C Ho, Anthony Bessios, Fred F Chen, Elad Alon, Mark A Horowitz. "United States Patent 10,411,923 High speed signaling system with adaptive transmit pre-emphasis", Rambus Inc, Sep 10, 2019
- Mark A Horowitz, Craig E Hampel, Alfredo Moncayo, Kevin S Donnelly, Jared L Zerbe. "United States Patent 10,366,045 Flash controller to provide a value that represents a parameter to a flash memory Inventors", Rambus Inc, Jul 30, 2019
- Noy Cohen, Marc S Levoy, Michael J Broxton, Logan Grosenick, Samuel Yang, Aaron Andalman, Karl A Disseroth, Mark A Horowitz. "United States Patent 10,317,597 Light-field microscopy with phase masking", Leland Stanford Junior University, Jun 11, 2019
- Jared LeVan Zerbe, Kevin S Donnelly, Stefanos Sidiropoulos, Donald C Stark, Mark A Horowitz, Leung Yu, Roxanne Vu, Jun Kim, Bruno W Garlepp, Tsyr-Chyang Ho, Benedict Chung-Kwong Lau. "United States Patent 10,310,999 Flash memory controller with calibrated data communication", Rambus Inc, Jun 4, 2019

- Jared L Zerbe, Bruno W Garlepp, Pak S Chau, Kevin S Donnelly, Mark A Horowitz, Stefanos Sidiropoulos, Billy W Garrett Jr, Carl W Werner. "United States Patent 9,998,305 Multi-PAM output driver with distortion compensation", Rambus Inc, Jun 12, 2018
- Haw-Jyh Liaw, Xingchao Yuan, Mark A Horowitz. "United States Patent 9,977,076 Technique for determining performance characteristics of electronic devices and systems", Rambus Inc, May 22, 2018
- Vladimir M Stojanovic, Andrew C Ho, Anthony Bessios, Bruno W Garlepp, Grace Tsang, Mark A Horowitz, Jared L Zerbe, Jason C Wei. "United States Patent 9,917,708 Partial response receiver", Rambus Inc, Mar 6, 2018

LINKS

- AHA! Agile Hardware Program: https://aha.stanford.edu/

Teaching

COURSES

2021-22

- An Intro to Making: What is EE: ENGR 40M (Aut, Win)
- An Intro to Making: What is EE: OSPBER 40M (Aut, Win)
- Digital Systems Engineering: EE 273 (Win)

2020-21

- An Intro to Making: What is EE: ENGR 40M (Aut, Spr)
- Digital Systems Engineering: EE 273 (Spr)
- Embedded Systems Workshop: EE 285 (Win)

2019-20

- An Intro to Making: What is EE: ENGR 40M (Aut, Win)
- An Intro to Making: What is EE: OSPBER 40M (Aut, Win)
- An Intro to Making: What is EE: OSPPARIS 40M (Aut)
- Design Projects in VLSI Systems: EE 272 (Win)
- Embedded Systems Workshop: CS 241, EE 285 (Win, Spr)
- Interactive Light Sculpture Project: EE 185 (Aut, Win, Spr)

STANFORD ADVISEES

Doctoral Dissertation Reader (AC)

Po-Han Chen, Timothy Chong, Kathleen Feng, West Foster, Jackson Melchert, Amr Mohamed, Aya Mouallem, Seung Je Woo

Doctoral Dissertation Advisor (AC)

Nikhil Bhagdikar, Alex Carsello, Sneha Goenka, Taeyoung Kong, Qiaoyi(Joey) Liu, Zachary Myers, Ankita Nayak, Gedeon Nyengele, Jeff Setter, Kavya Sreedhar, Daniel Stanley, Maxwell Strange, Sunil Sudhakaran, Can WANG

Orals Evaluator

Amr Mohamed

Master's Program Advisor

Annie Ho, Jake Ke, Liana Keesing, Anna Leong, Ann Wu, Jack Xiao, Shunyao Xu, Zhenbang You

Doctoral (Program)

Nikhil Bhagdikar, Anna Broome, Alex Carsello, Brandon D'Agostino, Qian Dong, Aidan Fitzpatrick, Teguh Hofstee, Lisa Lei, Zachary Myers, Ankita Nayak, Jeff Setter, Kavya Sreedhar, Daniel Stanley, Sunil Sudhakaran, Can WANG

Publications

PUBLICATIONS

- **AHA: An Agile Approach to the Design of Coarse-Grained Reconfigurable Accelerators and Compilers** *ACM Transactions on Embedded Computing Systems*
  Koul, K., Melchert, J., Sreedhar, K., Truong, L., Nyengele, G., Zhang, K., Liu, Q., Setter, J., Chen, P., Mei, Y., Strange, M., Daly, R., Donovick, et al
  2023; 22 (2)

- **Hardware Abstractions and Hardware Mechanisms to Support Multi-Task Execution on Coarse-Grained Reconfigurable Arrays** *arXiv*
  Kong, T., Koul, K., Raina, P., Horowitz, M., Torng, C.
  2023

- **Higher education's influence on social networks and entrepreneurship in Brazil** *SOCIAL NETWORK ANALYSIS AND MINING*
  Reddy, M., Nardelli, J. C., Pereira, Y. L., Oliveira, L. B., Silva, T. H., Vasconcelos, M., Horowitz, M.
  2022; 13 (1)

- **An Open-Source Framework for FPGA Emulation of Analog/Mixed-Signal Integrated Circuit Designs** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Herbst, S., Rutsch, G., Ecker, W., Horowitz, M.
  2022; 41 (7): 2223-2236

- **Improving Energy Efficiency of CGRAs with Low-Overhead Fine-Grained Power Domains** *ACM Transactions on Reconfigurable Technology and Systems*
  Nayak, A., Zhang, K., Setaluri, R., Carsello, A., Mann, M., Torng, C., Richardson, S., Bahr, R., Hanrahan, P., Horowitz, M., Raina, P.
  2022

- **Enabling and Accelerating Dynamic Vision Transformer Inference for Real-Time Applications** *arXiv*
  Sreedhar, K., Clemons, J., Venkatesan, R., Keckler, S. W., Horowitz, M.
  2022

- **Canal: A Flexible Interconnect Generator for Coarse-Grained Reconfigurable Arrays** *arXiv*
  Melchert, J., Zhang, K., Mei, Y., Horowitz, M., Torng, C., Raina, P.
  2022

- **Cascade: An Application Pipelining Toolkit for Coarse-Grained Reconfigurable Arrays** *arXiv*
  Melchert, J., Mei, Y., Koul, K., Liu, Q., Horowitz, M., Raina, P.
  2022

- **The Sparse Abstract Machine** *arXiv*
  Hsu, O., Strange, M., Won, J., Sharma, R., Olukotun, K., Emer, J., Horowitz, M., Kjolstad, F.
  2022

- **Amber: Coarse-Grained Reconfigurable Array-Based SoC for Dense Linear Algebra Acceleration** *2022 IEEE Hot Chips 34 Symposium (HCS)*
  Feng, K., et al
  2022: 1-30

- **mflowgen: a modular flow generator and ecosystem for community-driven physical design** *DAC '22: Proceedings of the 59th ACM/IEEE Design Automation Conference*
  Carsello, A., Thomas, J., Nayak, A., Chen, P., Horowitz, M., Raina, P., Torng, C.
  2022: 1339–1342

- **Bringing source-level debugging frameworks to hardware generators** *DAC '22: Proceedings of the 59th ACM/IEEE Design Automation Conference*
  Zhang, K., Asgar, Z., Horowitz, M.
  2022: 1171–1176

- **Amber: A 367 GOPS, 538 GOPS/W 16nm SoC with a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra** *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*
  Carsello, A., et al
  2022

- **Automating System Configuration** *CONFERENCE ON FORMAL METHODS IN COMPUTER-AIDED DESIGN–FMCAD 2021*

Tsiskaridze, N., Strange, M., Mann, M., Sreedhar, K., Liu, Q., Horowitz, M., Barrett, C.
2021

- **Online, Interactive Tool for Studying How Students Troubleshoot Circuits** *2021 ASEE Virtual Annual Conference*
  Fritz, A., Horowitz, M., Jha, A.
  2021

- **Compiling Halide Programs to Push-Memory Accelerators** *arXiv.org (https://arxiv.org/abs/2105.12858)*
  Liu, Q., Huff, D., Setter, J., Strange, M., Feng, K., Sreedhar, K., Wang, Z., Zhang, K., Horowitz, M., Raina, P., Kjolstad, F.
  2021

- **Automated Design Space Exploration of CGRA Processing Element Architectures using Frequent Subgraph Analysis** *arXiv.org (https://arxiv.org/abs/2104.14155)*
  Melchert, J., Feng, K., Donovick, C., Daly, R., Barrett, C., Horowitz, M., Hanrahan, P., Raina, P.
  2021

- **A Fast Large-Integer Extended GCD Algorithm and Hardware Design for Verifiable Delay Functions and Modular Inversion** *Cryptology ePrint Archive*
  Sreedhar, K., Horowitz, M., Torng, C.
  2021

- **Enabling Reusable Physical Design Flows with Modular Flow Generators** *arXiv.org*
  Carsello, A., Thomas, J., Nayak, A., Chen, P., Horowitz, M., Raina, P., Torng, C.
  2021

- **Fast Validation of Mixed-Signal SoCs** *IEEE Open Journal of the Solid-State Circuits Society*
  Stanley, D., Wang, C., Kim, S., Herbst, S., Kim, J., Horowitz, M.
  2021; 1: 184 - 195

- **fault: A Python Embedded Domain-Specific Language for Metaprogramming Portable Hardware Verification Components** *International Conference on Computer Aided Verification*
  Truong, L., Herbst, S., Setaluri, R., Mann, M., Daly, R., Zhang, K., Donovick, C., Stanley, D., Horowitz, M., Barrett, C., Hanrahan, P.
  2020

- **Interstellar: Using Halide's Scheduling Language to Analyze DNN Accelerators**
  Yang, X., Gao, M., Liu, Q., Setter, J., Pu, J., Nayak, A., Bell, S., Cao, K., Ha, H., Raina, P., Kozyrakis, C., Horowitz, M., ACM
  ASSOC COMPUTING MACHINERY.2020: 369–83

- **20-GS/s 8-bit Analog-to-Digital Converter and 5-GHz Phase Interpolator for Open-Source Synthesizable High-Speed Link Applications** *IEEE Solid-State Circuits Letters*
  Kim, S., Myers, Z., Herbst, S., Lim, B., Horowitz, M.
  2020; 3: 518 - 521

- **SegAlign: A Scalable GPU-Based Whole Genome Aligner** *International Conference for High Performance Computing, Networking, Storage and Analysis (SC)*
  Goenka, S., Turakhia, Y., Paten, B., Horowitz, M.
  2020: 540–552

- **Creating an Agile Hardware Design Flow** *2020 57th ACM/IEEE Design Automation Conference (DAC)*
  Bahr, R., Barrett, C., Bhagdikar, N., Carsello, A., Daly, R., Donovick, C., Durst, D., Fatahalian, K., Feng, K., Hanrahan, P., Hofstee, T., Horowitz, M., Huff, et al
  2020

- **A Framework for Adding Low-Overhead, Fine-Grained Power Domains to CGRAs**
  Nayak, A., Zhang, K., Setaluri, R., Carsello, A., Mann, M., Richardson, S., Bahr, R., Hanrahan, P., Horowitz, M., Raina, P.
  Design, Automation and Test in Europe Conference (DATE).
  2020

- **Open-Source Synthesizable Analog Blocks for High-Speed Link Designs: 20-GS/s 5b ENOB Analog-to-Digital Converter and 5-GHz Phase Interpolator** *2020 IEEE Symposium on VLSI Circuits*
  Kim, S., Myers, Z., Herbst, S., Lim, B., Horowitz, M.
  2020

- **An Analog Model Template Library: Simplifying Chip-Level, Mixed-Signal Design Verification** *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS*
  Lim, B., Horowitz, M.
  2019; 27 (1): 193–204
- **TANGRAM: Optimized Coarse-Grained Dataflow for Scalable NN Accelerators** *ASPLOS '19: Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems*
  Gao, M., Yang, X., Pu, J., Horowitz, M., Kozyrakis, C.
  2019: 807–20
- **StartupBR: Higher Education's Influence on Social Networks and Entrepreneurship in Brazil** *arXiv:1904.12026*
  Reddy, M., Nardelli, J. C., Pereira, Y. L., Vasconcelos, M., Silva, T. H., Oliveira, L. B., Horowitz, M.
  2019
- **DATASET CULLING: TOWARDS EFFICIENT TRAINING OF DISTILLATION-BASED DOMAIN SPECIFIC MODELS**
  Yoshioka, K., Lee, E., Wong, S., Horowitz, M., IEEE
  IEEE.2019: 3237–41
- **Trapped Ion Quantum Computers** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Grumbling, E., Horowitz, M., Comm Tech Assessment Feasibility, Comp Sci Telecommun Board, Intelligence Community Studies Boa, Div Engn Phys Sci, Natl Acad Sci Engn Med, Grumbling, E., Horowitz, M.
  2019: 196–204
- **Feasibility and Time Frames of Quantum Computing** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: 156–92
- **Progress in Computing** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: 12–23
- **QUANTUM COMPUTING Progress and Prospects Preface** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: XI-XV
- **Superconducting Quantum Computers** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: 205–11
- **Quantum Computing's Implications for Cryptography** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: 95–112
- **Quantum Algorithms and Applications** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: 57–94
- **QUANTUM COMPUTING Progress and Prospects Summary** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: 1–11
- **Other Approaches to Building Qubits** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al

2019: 212–25

- **Statement of Task** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: 195
- **Essential Hardware Components of a Quantum Computer** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: 113–34
- **Essential Software Components of a Scalable Quantum Computer** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: 135–55
- **Global R&D Investment** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: 226–29
- **Quantum Computing: A New Paradigm** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  2019: 24–56
- **Falcon — A Flexible Architecture For Accelerating Cryptography** *2019 IEEE 16th International Conference on Mobile Ad Hoc and Sensor Systems (MASS)*
  Kiningham, K., Levis, P., Anderson, M., Boneh, D., Horowitz, M., Shih, M.
  2019
- **Mapping Histological Slice Sequences to the Allen Mouse Brain Atlas Without 3D Reconstruction.** *Frontiers in neuroinformatics*
  Xiong, J., Ren, J., Luo, L., Horowitz, M.
  2018; 12: 93
- **Mapping Histological Slice Sequences to the Allen Mouse Brain Atlas Without 3D Reconstruction** *FRONTIERS IN NEUROINFORMATICS*
  Xiong, J., Ren, J., Luo, L., Horowitz, M.
  2018; 12
- **Anatomically Defined and Functionally Distinct Dorsal Raphe Serotonin Sub-systems** *CELL*
  Ren, J., Friedmann, D., Xiong, J., Liu, C. D., Ferguson, B. R., Weerakkody, T., DeLoach, K. E., Ran, C., Pun, A., Sun, Y., Weissbourd, B., Neve, R. L., Huguenard, et al
  2018; 175 (2): 472-+
- **The Interaction Engine** *DESIGN THINKING RESEARCH: MAKING DISTINCTIONS: COLLABORATION VERSUS COOPERATION*
  Martelaro, N., Ju, W., Horowitz, M., Plattner, H., Meinel, C., Leifer, L.
  2018: 147–69
- **Tethys: Collecting Sensor Data without Infrastracture or Trust** *2018 IEEE/ACM Third International Conference on Internet-of-Things Design and Implementation (IoTDI)*
  Chiang, H., Hong, J., Kiningham, K., Riliskis, L., Levis, P., Horowitz, M.
  2018: 249–54
- **Rethinking Non-major Circuits Pedagogy for Improved Motivation**
  Bell, S., Horowitz, M.
  2018 ASEE Annual Conference & Exposition (https://peer.asee.org/30936).
  2018
- **DNN Dataflow Choice Is Overrated** *arXiv:1809.04070*
  Yang, X., Gao, M., Pu, J., Nayak, A., Liu, Q., Bell, S. E., Setter, J. O., Cao, K., Ha, H., Kozyrakis, C., Horowitz, M.
  2018

- **Training Domain Specific Models for Energy-Efficient Object Detection** *arXiv:1811.02689*
  Yoshioka, K., Lee, E., Horowitz, M.
  2018
- **Compiling Algorithms for Heterogeneous Systems** *Synthesis Lectures on Computer Architecture*
  Bell, S., Pu, J., Hegarty, J., Horowitz, M.
  2018: 105
- **Mapping Mouse Brain Slice Sequence to a Reference Brain Without 3D Reconstruction** *bioRxiv*
  Xiong, J., Ren, J., Luo, L., Horowitz, M.
  2018
- **Fast FPGA Emulation of Analog Dynamics in Digitally-Driven Systems**
  Herbst, S., Lim, B., Horowitz, M., Assoc Comp Machinery
  ASSOC COMPUTING MACHINERY.2018
- **Anatomically Defined and Functionally Distinct Dorsal Raphe Serotonin Sub-systems.** *Cell*
  Ren, J. n., Friedmann, D. n., Xiong, J. n., Liu, C. D., Ferguson, B. R., Weerakkody, T. n., DeLoach, K. E., Ran, C. n., Pun, A. n., Sun, Y. n., Weissbourd, B. n., Neve, R. L., Huguenard, et al
  2018
- **Volumetric Image Registration From Invariant Keypoints** *IEEE TRANSACTIONS ON IMAGE PROCESSING*
  Rister, B., Horowitz, M. A., Rubin, D. L.
  2017; 26 (10): 4900–4910
- **Scalable Device for Automated Microbial Electroporation in a Digital Microfluidic Platform.** *ACS synthetic biology*
  Madison, A. C., Royal, M. W., Vigneault, F., Chen, L., Griffin, P. B., Horowitz, M., Church, G. M., Fair, R. B.
  2017; 6 (9): 1701-1709
- **Programming Heterogeneous Systems from an Image Processing DSL** *ACM TRANSACTIONS ON ARCHITECTURE AND CODE OPTIMIZATION*
  Pu, J., Bell, S., Yang, X., Setter, J., Richardson, S., Ragan-Kelley, J., Horowitz, M.
  2017; 14 (3)
- **Dynamic structure of locomotor behavior in walking fruit flies** *ELIFE*
  Katsov, A. Y., Freifeld, L., Horowitz, M., Kuehn, S., Clandinin, T. R.
  2017; 6
- **Microfluidic-based mini-metagenomics enables discovery of novel microbial lineages from complex environmental samples** *ELIFE*
  Yu, F., Blainey, P. C., Schulz, F., Woyke, T., Horowitz, M. A., Quake, S. R.
  2017; 6
- **Local inhibition of microtubule dynamics by dynein is required for neuronal cargo distribution** *NATURE COMMUNICATIONS*
  Yogev, S., Maeder, C. I., Cooper, R., Horowitz, M., Hendricks, A. G., Shen, K.
  2017; 8
- **Dark Memory and Accelerator-Rich System Optimization in the Dark Silicon Era** *IEEE DESIGN & TEST*
  Pedram, A., Richardson, S., Horowitz, M., Galal, S., Kvatinsky, S.
  2017; 34 (2): 39-50
- **TETRIS: Scalable and Efficient Neural Network Acceleration with 3D Memory**
  Gao, M., Pu, J., Yang, X., Horowitz, M., Kozyrakis, C.
  ASSOC COMPUTING MACHINERY.2017: 751-764
- **TETRIS: Scalable and Efficient Neural Network Acceleration with 3D Memory** *ACM SIGPLAN NOTICES*
  Gao, M., Pu, J., Yang, X., Horowitz, M., Kozyrakis, C.
  2017; 52 (4): 751-764
- **Long-term microfluidic tracking of coccoid cyanobacterial cells reveals robust control of division timing** *BMC BIOLOGY*
  Yu, F. B., Willis, L., Chau, R. M., Zambon, A., Horowitz, M., Bhaya, D., Huang, K. C., Quake, S. R.
  2017; 15

- **Microtubule Organization Determines Axonal Transport Dynamics.** *Neuron*
  Yogev, S., Cooper, R., Fetter, R., Horowitz, M., Shen, K.
  2016; 92 (2): 449-460
- **Rigel: Flexible Multi-Rate Image Processing Hardware** *ACM TRANSACTIONS ON GRAPHICS*
  Hegarty, J., Daly, R., DeVito, Z., Ragan-Kelley, J., Horowitz, M., Hanrahan, P.
  2016; 35 (4)
- **Tomographic Reconstruction and Alignment Using Matrix Norm Minimization** *IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING*
  Song, K., Horowitz, M.
  2016; 10 (1): 47-60
- **Error Control and Limit Cycle Elimination in Event-Driven Piecewise Linear Analog Functional Models** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS*
  Lim, B. C., Horowitz, M.
  2016; 63 (1): 23-33
- **A 220pJ/Pixel/Frame CMOS Image Sensor with Partial Settling Readout Architecture**
  Ji, S., Pu, J., Lim, B., Horowitz, M., IEEE
  IEEE.2016
- **EIE: Efficient Inference Engine on Compressed Deep Neural Network**
  Han, S., Liu, X., Mao, H., Pu, J., Pedram, A., Horowitz, M. A., Dally, W. J., IEEE
  IEEE.2016: 243-254
- **Evaluating Programmable Architectures for Imaging and Vision Applications**
  Vasilyev, A., Bhagdikar, N., Pedram, A., Richardson, S., Kvatinsky, S., Horowitz, M., IEEE
  IEEE.2016
- **Deep Compression and EIE: Efficient Inference Engine on Compressed Deep Neural Network**
  Han, S., Liu, X., Mao, H., Pu, J., Pedram, A., Horowitz, M., Daily, B., IEEE
  IEEE.2016
- **Improving Energy Efficiency of DRAM by Exploiting Half Page Row Access**
  Ha, H., Pedram, A., Richardson, S., Kvatinsky, S., Horowitz, M., IEEE
  IEEE.2016
- **Convolution Engine: Balancing Efficiency and Flexibility in Specialized Computing** *COMMUNICATIONS OF THE ACM*
  Qadeer, W., Hameed, R., Shacham, O., Venkatesan, P., Kozyrakis, C., Horowitz, M.
  2015; 58 (4): 85-93
- **Building Conflict-Free FFT Schedules** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS*
  Richardson, S., Markovic, D., Danowitz, A., Brunhaver, J., Horowitz, M.
  2015; 62 (4): 1146-1155
- **Digital Analog Design: Enabling Mixed-Signal System Validation** *IEEE DESIGN & TEST*
  Lim, B. C., Mao, J., Horowitz, M., Jang, J., Kim, J.
  2015; 32 (1): 44-52
- **Demo Abstract: Tethys - An Energy Harvesting Networked Water Flow Sensor**
  Chiang, H., Hong, J., Kiningham, K., Xue, J., Riliskis, L., Levis, P., Horowitz, M., ACM
  ASSOC COMPUTING MACHINERY.2015: 489-490
- **SCALE- AND ORIENTATION-INVARIANT KEYPOINTS IN HIGHER-DIMENSIONAL DATA**
  Rister, B., Reiter, D., Zhang, H., Volz, D., Horowitz, M., Gabrt, R. E., Cavallaro, J. R., IEEE
  IEEE.2015: 3490-3494
- **Enhancing the performance of the light field microscope using wavefront coding** *OPTICS EXPRESS*
  Cohen, N., Yang, S., Andalman, A., Broxton, M., Grosenick, L., Deisseroth, K., Horowitz, M., Levoy, M.
  2014; 22 (20): 24817-24839

- **A Verilog Piecewise-Linear Analog Behavior Model for Mixed-Signal Validation** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS*
  Liao, S., Horowitz, M.
  2014; 61 (8): 2229-2235
- **Darkroom: Compiling High-Level Image Processing Code into Hardware Pipelines** *ACM TRANSACTIONS ON GRAPHICS*
  Hegarty, J., Brunhaver, J., DeVito, Z., Ragan-Kelley, J., Cohen, N., Bell, S., Vasilyev, A., Horowitz, M., Hanrahan, P.
  2014; 33 (4)
- **Large-scale mapping of transposable element insertion sites using digital encoding of sample identity.** *Genetics*
  Gohl, D. M., Freifeld, L., Silies, M., Hwa, J. J., Horowitz, M., Clandinin, T. R.
  2014; 196 (3): 615-623
- **Large-scale mapping of transposable element insertion sites using digital encoding of sample identity.** *Genetics*
  Gohl, D. M., Freifeld, L., Silies, M., Hwa, J. J., Horowitz, M., Clandinin, T. R.
  2014; 196 (3): 615-623
- **Computing's Energy Problem (and what we can do about it)**
  Horowitz, M., IEEE
  IEEE.2014: 10-14
- **Forwarding Metamorphosis: Fast Programmable Match-Action Processing in Hardware for SDN** *SIGCOMM Conference*
  Bosshart, P., Gibb, G., Kim, H., Varghese, G., McKeown, N., Izzard, M., Mujica, F., Horowitz, M.
  ASSOC COMPUTING MACHINERY.2013: 99–110
- **GABAergic Lateral Interactions Tune the Early Stages of Visual Processing in Drosophila** *NEURON*
  Freifeld, L., Clark, D. A., Schnitzer, M. J., Horowitz, M. A., Clandinin, T. R.
  2013; 78 (6): 1075-1089
- **Microfluidic serial digital to analog pressure converter for arbitrary pressure generation and contamination-free flow control** *LAB ON A CHIP*
  Yu, F., Horowitz, M. A., Quake, S. R.
  2013; 13 (10): 1911-1918
- **A Verilog Piecewise-Linear Analog Behavior Model for Mixed-Signal Validation** *35th Annual IEEE Custom Integrated Circuits Conference (CICC) - The Showcase for Circuit Design in the Heart of Silicon Valley*
  Liao, S., Horowitz, M.
  IEEE.2013
- **Design Principles for Packet Parsers** *9th ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS)*
  Gibb, G., Varghese, G., Horowitz, M., McKeown, N.
  IEEE.2013: 13–24
- **An Area-Efficient Minimum-Time FFT Schedule Using Single-Ported Memory** *IFIP/IEEE 21st International Conference on Very Large Scale Integration (VLSI-SoC)*
  Richardson, S., Shacham, O., Markovic, D., Horowitz, M.
  IEEE.2013: 39–44
- **FPU Generator for Design Space Exploration** *21st IEEE Symposium on Computer Arithmetic (ARITH)*
  Galal, S., Shacham, O., Brunhaver, J. S., Pu, J., Vassiliev, A., Horowitz, M.
  IEEE.2013: 25–34
- **The Frankencamera: An Experimental Platform for Computational Photography** *COMMUNICATIONS OF THE ACM*
  Adams, A., Jacobs, D. E., Dolson, J., Tico, M., Pulli, K., Talvala, E., Ajdin, B., Vaquero, D., Lensch, H. P., Horowitz, M., Park, S. H., Gelfand, N., Baek, et al
  2012; 55 (11): 90-98
- **Bringing Up a Chip on the Cheap** *IEEE DESIGN & TEST OF COMPUTERS*
  Wachs, M., Shacham, O., Asgar, Z., Firoozshahian, A., Richardson, S., Horowitz, M.
  2012; 29 (6): 57-65
- **Removing high contrast artifacts via digital inpainting in cryo-electron tomography: An application of compressed sensing** *JOURNAL OF STRUCTURAL BIOLOGY*

Song, K., Comolli, L. R., Horowitz, M.
2012; 178 (2): 108-120

- **CMOS Image Sensors With Multi-Bucket Pixels for Computational Photography** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Wan, G., Li, X., Agranov, G., Levoy, M., Horowitz, M.
  2012; 47 (4): 1031-1042

- **CPU DB: Recording Microprocessor History** *COMMUNICATIONS OF THE ACM*
  Danowitz, A., Kelley, K., Mao, J., Stevenson, J. P., Horowitz, M.
  2012; 55 (4): 55-63

- **Avoiding Game Over: Bringing Design to the Next Level** *49th ACM/EDAC/IEEE Design Automation Conference (DAC)*
  Shacham, O., Galal, S., Sankaranarayanan, S., Wachs, M., Brunhaver, J., Vassiliev, A., Horowitz, M., Danowitz, A., Qadeer, W., Richardson, S.
  IEEE.2012: 623–629

- **A New IC with Level-Crossing ADC Readout Architecture for PET Detector Signals** *IEEE Nuclear Science Symposium / Medical Imaging Conference Record (NSS/MIC) / 19th Room-Temperature Semiconductor X-ray and Gamma-ray Detector Workshop*
  Lau, F. W., Choi, H. H., Horowitz, M. A., Levin, C. S.
  IEEE.2012: 2486–2488

- **Design Automation Framework for Application-Specific Logic-in-Memory Blocks** *23rd IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)*
  Zhu, Q., Vaidyanathan, K., Shacham, O., Horowitz, M., Pileggi, L., Franchetti, F.
  IEEE.2012: 125–132

- **Rethinking DRAM Power Modes for Energy Proportionality** *45th IEEE/ACM Annual International Symposium on Microarchitecture (MICRO)*
  Malladi, K. T., Shaeffer, I., Gopalakrishnan, L., Lo, D., Lee, B. C., Horowitz, M.
  IEEE COMPUTER SOC.2012: 131–142

- **Removing Overhead From High-Level Interfaces** *49th ACM/EDAC/IEEE Design Automation Conference (DAC)*
  Kelly, K., Wachs, M., Stevenson, J., Richardson, S., Horowitz, M.
  IEEE.2012: 783–789

- **Towards Energy-Proportional Datacenter Memory with Mobile DRAM** *39th Annual International Symposium on Computer Architecture (ISCA)*
  Malladi, K. T., Nothaft, F. A., Periyathambi, K., Lee, B. C., Kozyrakis, C., Horowitz, M.
  IEEE.2012: 37–48

- **Understanding Sources of Inefficiency in General-Purpose Chips** *COMMUNICATIONS OF THE ACM*
  Hameed, R., Qadeer, W., Wachs, M., Azizi, O., Solomatnikov, A., Lee, B. C., Richardson, S., Kozyrakis, C., Horowitz, M.
  2011; 54 (10): 85-93

- **Energy-Efficient Floating-Point Unit Design** *IEEE TRANSACTIONS ON COMPUTERS*
  Galal, S., Horowitz, M.
  2011; 60 (7): 913-922

- **Defining the Computational Structure of the Motion Detector in Drosophila** *NEURON*
  Clark, D. A., Bursztyn, L., Horowitz, M. A., Schnitzer, M. J., Clandinin, T. R.
  2011; 70 (6): 1165-1177

- **Cortical representations of olfactory input by trans-synaptic tracing** *NATURE*
  Miyamichi, K., Amat, F., Moussavi, F., Wang, C., Wickersham, I., Wall, N. R., Taniguchi, H., Tasic, B., Huang, Z. J., He, Z., Callaway, E. M., Horowitz, M. A., Luo, et al
  2011; 472 (7342): 191-196

- **Latency Sensitive FMA Design** *20th IEEE Symposium on Computer Arithmetic (ARITH)*
  Galal, S., Horowitz, M.
  IEEE COMPUTER SOC.2011: 129–138

- **Intermediate Representations for Controllers in Chip Generators**
  Kelley, K., Wachs, M., Danowitz, A., Stevenson, P., Richardon, S., Horowitz, M., IEEE
  IEEE.2011: 1394-1399

- **Joint DAC/IWBDA Special Session Design and Synthesis of Biological Circuits** *48th ACM/IEEE/EDAC Design Automation Conference (DAC)*
  Densmore, D., Horowitz, M., Krishnaswamy, S., Shen, X., Arkin, A., Winfree, E., Voigt, C.
  ASSOC COMPUTING MACHINERY.2011: 114–115
- **Global Convergence Analysis of Mixed-Signal Systems** *48th ACM/IEEE/EDAC Design Automation Conference (DAC)*
  Youn, S., Kim, J., Horowitz, M.
  ASSOC COMPUTING MACHINERY.2011: 498–503
- **Global convergence analysis of mixed-signal systems** *Design Automation Conference (DAC)*
  Youn, S., Kim, J., Horowitz, M.
  2011: 498-503
- **Energy-efficient floating point unit design** *Computers, IEEE Transactions on*
  Galal, S., Horowitz, M.
  2011; 99: 1-1
- **Analog signal multiplexing for PSAPD-based PET detectors: simulation and experimental validation** *PHYSICS IN MEDICINE AND BIOLOGY*
  Lau, F. W., Vandenbroucke, A., Reynolds, P. D., Olcott, P. D., Horowitz, M. A., Levin, C. S.
  2010; 55 (23): 7149-7174
- **Analysis of the Intact Surface Layer of Caulobacter crescentus by Cryo-Electron Tomography** *JOURNAL OF BACTERIOLOGY*
  Amat, F., Comolli, L. R., Nomellini, J. F., Moussavi, F., Downing, K. H., Smit, J., Horowitz, M.
  2010; 192 (22): 5855-5865
- **RETHINKING DIGITAL DESIGN: WHY DESIGN MUST CHANGE** *IEEE MICRO*
  Shacham, O., Azizi, O., Wachs, M., Qadeer, W., Asgar, Z., Kelley, K., Stevenson, J. P., Richardson, S., Horowitz, M., Lee, B., Solomatnikov, A., Firoozshahian, A.
  2010; 30 (6): 9-24
- **Subtomogram alignment by adaptive Fourier coefficient thresholding** *JOURNAL OF STRUCTURAL BIOLOGY*
  Amat, F., Comolli, L. R., Moussavi, F., Smit, J., Downing, K. H., Horowitz, M.
  2010; 171 (3): 332-344
- **The Frankencamera: An Experimental Platform for Computational Photography** *ACM TRANSACTIONS ON GRAPHICS*
  Adams, A., Jacobs, D. E., Dolson, J., Tico, M., Pulli, K., Talvala, E., Ajdin, B., Vaquero, D., Lensch, H. P., Horowitz, M., Park, S. H., Gelfand, N., Baek, et al
  2010; 29 (4)
- **Fast, Non-Monte-Carlo Estimation of Transient Performance Variation Due to Device Mismatch** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS*
  Kim, J., Jones, K. D., Horowitz, M. A.
  2010; 57 (7): 1746-1755
- **3D segmentation of cell boundaries from whole cell cryogenic electron tomography volumes** *JOURNAL OF STRUCTURAL BIOLOGY*
  Moussavi, F., Heitz, G., Amat, F., Comolli, L. R., Koller, D., Horowitz, M.
  2010; 170 (1): 134-145
- **Static control logic for microfluidic devices using pressure-gain valves** *NATURE PHYSICS*
  Weaver, J. A., Melin, J., Stark, D., Quake, S. R., Horowitz, M. A.
  2010; 6 (3): 218-223
- **Timing Robustness in the Budding and Fission Yeast Cell Cycles** *PLOS ONE*
  Mangla, K., Dill, D. L., Horowitz, M. A.
  2010; 5 (2)
- **Energy-Performance Tradeoffs in Processor Architecture and Circuit Design: A Marginal Cost Analysis** *37th International Symposium on Computer Architecture*
  Azizi, O., Mahesri, A., Lee, B. C., Patel, S. J., Horowitz, M.
  ASSOC COMPUTING MACHINERY.2010: 26–36
- **Fortifying Analog Models with Equivalence Checking and Coverage Analysis**
  Horowitz, M., Jeeradit, M., Lau, F., Liao, S., Lim, B., Mao, J., IEEE

IEEE.2010: 425-430

- **An Integrated Framework for Joint Design Space Exploration of Microarchitecture and Circuits**
  Azizi, O., Mahesri, A., Stevenson, J. P., Patel, S. J., Horowitz, M., IEEE
  IEEE.2010: 250-255
- **Why Design Must Change: Rethinking Digital Design**
  Horowitz, M., IEEE
  IEEE.2010: 791
- **An Efficient Test Vector Generation for Checking Analog/Mixed-Signal Functional Models**
  Lim, B., Kim, J., Horowitz, M. A., IEEE
  IEEE.2010: 767–72
- **Intent-Leveraged Optimization of Analog Circuits via Homotopy**
  Jeeradit, M., Kim, J., Horowitz, M., IEEE
  IEEE.2010: 1614–19
- **Chapter Thirteen-Alignment of Cryo-Electron Tomography Datasets** *Methods in enzymology*
  Amat, F., Castaño-Diez, D., Lawrence, A., Moussavi, F., Winkler, H., Horowitz, M.
  Elsevier.2010: 343–367
- **2010 Timing Robustness in the Budding and Fission Yeast Cell Cycles.** *PLoS ONE*
  K, M., DL, D., A, H. M.
  2010; 2 (5): e8906
- **An integrated framework for joint design space exploration of microarchitecture and circuits**
  Azizi, O., Mahesri, A., Stevenson, J., P., Patel, S., J., Horowitz, M.
  2010
- **An efficient test vector generation for checking analog/mixed-signal functional models**
  Lim, B., C., Kim, J., Horowitz, M., A.
  2010
- **Intent-leveraged optimization of analog circuits via homotopy**
  Jeeradit, M., Kim, J., Horowitz, M.
  2010
- **Fortifying analog models with equivalence checking and coverage analysis**
  Horowitz, M., Jeeradit, M., Lau, F., Liao, S., Lim, B., Mao, J.
  2010
- **ALIGNMENT OF CRYO-ELECTRON TOMOGRAPHY DATASETS** *METHODS IN ENZYMOLOGY, VOL 482: CRYO-EM, PART B: 3-D RECONSTRUCTION*
  Amat, F., Castano-Diez, D., Lawrence, A., Moussavi, F., Winkler, H., Horowitz, M.
  2010; 482: 343-367
- **Understanding Sources of Inefficiency in General-Purpose Chips** *37th International Symposium on Computer Architecture*
  Hameed, R., Qadeer, W., Wachs, M., Azizi, O., Solomatnikov, A., Lee, B. C., Richardson, S., Kozyrakis, C., Horowitz, M.
  ASSOC COMPUTING MACHINERY.2010: 37–47
- **Energy-Performance Tunable Logic** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Nezamfar, B., Alon, E., Horowitz, M.
  2009; 44 (9): 2554-2567
- **On-Die Power Supply Noise Measurement Techniques** *IEEE TRANSACTIONS ON ADVANCED PACKAGING*
  Alon, E., Abramzon, V., Nezamfar, B., Horowitz, M.
  2009; 32 (2): 248-259
- **Detector and front-end electronics for 1mm(3) resolution breast-dedicated PET system**
  Lau, F., Vandenbroucke, A., Reynolds, P., Olcott, P., Horowitz, M., Levin, C.

SOC NUCLEAR MEDICINE INC.2009

- **1 mm(3) Resolution Breast-Dedicated PET System** *IEEE Nuclear Science Symposium/Medical Imaging Conference*
  Lau, F. W., Fang, C., Reynolds, P. D., Olcott, P. D., Vandenbroucke, A., Spanoudaki, V. C., Olutade, F., Horowitz, M. A., Levin, C. S.
  IEEE.2009: 5378–5381
- **Using a configurable processor generator for computer architecture prototyping**
  Solomatnikov, A., Firoozshahian, A., Shacham, O., Asgar, Z., Wachs, M., Qadeer, W., Horowitz, M. A.
  2009
- **Area-efficiency in CMP core design: co-optimization of microarchitecture and physical design** *SIGARCH Comput. Archit. New*
  Azizi, O., Mahesri, A., Patel, S., J., Horowitz, M.
  2009; 37 (2): 56-65
- **Energy-Performance Tunable Logic** *IEEE Custom Integrated Circuits Conference*
  Nezamfar, B., Horowitz, M.
  IEEE.2009: 183–186
- **A Memory System Design Framework: Creating Smart Memories** *36th Annual International Symposium on Computer Architecture*
  Firoozshahian, A., Solomatnikov, A., Shacham, O., Asgar, Z., Richardson, S., Kozyrakis, C., Horowitz, M.
  ASSOC COMPUTING MACHINERY.2009: 406–417
- **Front-End Electronics for a 1 mm(3) Resolution Avalanche Photodiode-Based PET System with Analog Signal Multiplexing** *IEEE Nuclear Science Symposium/Medical Imaging Conference*
  Lau, F. W., Vandenbroucke, A., Reynolds, P. D., Olcott, P. D., Horowitz, M. A., Levin, C. S.
  IEEE.2009: 3146–3149
- **IN FIELD, ENERGY-PERFORMANCE TUNABLE FPGA ARCHITECTURES** *19th International Conference on Field Programmable Logic and Applications*
  Nezamfar, B., Horowitz, M.
  IEEE.2009: 262–267
- **Stochastic Steady-State and AC Analyses of Mixed-Signal Systems** *46th ACM/IEEE Design Automation Conference (DAC 2009)*
  Kim, J., Ren, J., Horowitz, M. A.
  IEEE.2009: 376–381
- **Leveraging Designer's Intent: A Path Toward Simpler Analog CAD Tools** *IEEE Custom Integrated Circuits Conference*
  Kim, J., Jeeradit, M., Lim, B., Horowitz, M. A.
  IEEE.2009: 613–620
- **Comparative Evaluation of Memory Models for Chip Multiprocessors** *ACM TRANSACTIONS ON ARCHITECTURE AND CODE OPTIMIZATION*
  Leverich, J., Arakida, H., Solomatnikov, A., Firoozshahian, A., Horowitz, M., Kozyrakis, C.
  2008; 5 (3)
- **Architecture and inherent robustness of a bacterial cell-cycle control system** *PROCEEDINGS OF THE NATIONAL ACADEMY OF SCIENCES OF THE UNITED STATES OF AMERICA*
  Shen, X., Collier, J., Dill, D., Shapiro, L., Horowitz, M., McAdams, H. H.
  2008; 105 (32): 11340-11345
- **Integrated regulation for energy-efficient digital circuits** *IEEE Custom Integrated Circuits Conference*
  Alon, E., Horowitz, M.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2008: 1795–1807
- **A 90 nm CMOS 16 Gb/s transceiver for optical interconnects** *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*
  Palermo, S., Emami-Neyestanak, A., Horowitz, M.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2008: 1235–46
- **Digital circuit design trends** *20th Symposium on VLSI Circuits*
  Horowitz, M., Stark, D., Alon, E.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2008: 757–61

- **A 24 Gb/s software programmable analog multi-tone transmitter** *20th Symposium on VLSI Circuits*
  Amirkhany, A., Abbasfar, A., Savoj, J., Jeeradit, M., Garlepp, B., Kollipara, R. T., Stojanovic, V., Horowitz, M.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2008: 999–1009
- **Markov random field based automatic image alignment for electron tomography** *4th International Conference on Electron Tomography*
  Amat, F., Moussavi, F., Comolli, L. R., Elidan, G., Downing, K. H., Horowitz, M.
  ACADEMIC PRESS INC ELSEVIER SCIENCE.2008: 260–75
- **Verification of Chip Multiprocessor Memory Systems Using A Relaxed Scoreboard** *41st Annual IEEE/ACM International Symposium on Microarchitecture*
  Shacham, O., Wachs, M., Solomatnikov, A., Firoozshahian, A., Richardson, S., Horowitz, M.
  IEEE COMPUTER SOC.2008: 294–305
- **Circuit-Level Requirements for MOSFET-Replacement Devices** *IEEE International Electron Devices Meeting*
  Kam, H., King-Liu, T., Alon, E., Horowitz, M.
  IEEE.2008: 427–427
- **The case for simple, visible cache coherency**
  Kunz, R., Horowitz, M.
  2008
- **Circuit-level requirements for MOSFET-replacement devices** *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*
  Kam, H., King-Liu, T., Alon, E., Horowitz, M.
  2008: 1-1
- **Markov random field based automatic image alignment for electron tomography** *Journal of Structural Biology*
  Amat, F., Moussavi, F., Comolli, L., R., Elidan, G., Downing et al, K., H.
  2008; 161 (3): 260-75
- **A High-speed, Low-power 3D-SRAM Architecture** *IEEE Custom Integrated Circuits Conference*
  Nho, H. H., Horowitz, M., Wong, S. S.
  IEEE.2008: 201–204
- **Processor performance modeling using symbolic simulation** *IEEE International Symposium on Performance Analysis of Systems and Software*
  Azizi, O., Collins, J., Patil, D., Wang, H., Horowitz, M.
  IEEE COMPUTER SOC.2008: 127–138
- **A 14-mW 6.25-Gb/s transceiver in 90-nm CMOS** *IEEE International Solid-State Circuits Conference (ISSCC)*
  Poulton, J., Palmer, R., Fuller, A. M., Greer, T., Eyles, J., Dally, W. J., Horowitz, M.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2007: 2745–57
- **An optical interconnect transceiver at 1550 nm using low-voltage electroabsorption modulators directly integrated to CMOS** *JOURNAL OF LIGHTWAVE TECHNOLOGY*
  Roth, J. E., Palermo, S., Helman, N. C., Bour, D. P., Miller, D. A., Horowitz, M.
  2007; 25 (12): 3739-3747
- **A heuristic for optimizing stochastic activity networks with applications to statistical digital circuit sizing** *OPTIMIZATION AND ENGINEERING*
  Kim, S., Boyd, S. P., Yun, S., Patil, D. D., Horowitz, M. A.
  2007; 8 (4): 397-430
- **Veiling glare in high dynamic range imaging** *ACM SIGGRAPH 2007 Conference*
  Talvala, E., Adams, A., Horowitz, M., Levoy, M.
  ASSOC COMPUTING MACHINERY.2007
- **Power optimization for SRAM and its scaling** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Morifuji, E., Patil, D., Horowitz, M., Nishi, Y.
  2007; 54 (4): 715-722
- **Chip multi-processor generator** *44th ACM/IEEE Design Automation Conference*
  Solomatnikov, A., Firoozshahian, A., Qadeer, W., Shacham, O., Kelley, K., Asgar, Z., Wachs, M., Hameed, R., Horowitz, M.
  IEEE.2007: 262–263

- **Variable domain transformation for linear PAC analysis of mixed-signal systems** *IEEE/ACM International Conference on Computer-Aided Design*
  Kim, J., Jones, K. D., Horowitz, M. A.
  IEEE.2007: 887–894
- **Fast, non-monte-carlo estimation of transient performance variation due to device mismatch** *44th ACM/IEEE Design Automation Conference*
  Kim, J., Jones, K. D., Horowitz, M. A.
  IEEE.2007: 440–443
- **Integrated regulation for energy-efficient digital circuits** *IEEE Custom Integrated Circuits Conference*
  Alon, E., Horowitz, M.
  IEEE.2007: 389–392
- **Variable domain transformation for linear PAC analysis of mixed-signal systems**
  Kim, J., Jones, K., D., Horowitz, M., A.
  2007
- **Fast, Non-Monte-Carlo Estimation of Transient Performance Variation Due to Device Mismatch**
  Kim, J., Jones, K., D., Horowitz, M., A.
  2007
- **1550nm Optical Interconnect Transceiver with Low Voltage Electroabsorption Modulators Flip-Chip Bonded to 90nm CMOS**
  Roth, J., E., Palermo, S., Helman, N., C., Bour, D., P., Miller, D., A. B., Horowitz, M.
  2007
- **Chip Multi-Processor Generator.** *DAC*
  Solomatnikov, A., Firoozshahian, A., Qadeer, W., Shacham, O., Kelley, K., Asgar, Z., Horowitz, M. A.
  2007
- **Integrated Regulation for Energy-Efficient Digital Circuits**
  Alon, E., Horowitz, M.
  2007
- **A 24Gbps Software Programmable Multi-Channel Transmitter**
  Amirkhany, A., Abbasfar, A., Savoj, J., Jeeradit, M., Garlepp, B., Stojanovic, V., Horowitz, M. A.
  2007
- **A 12GS/S Phase-Calibrated CMOS Digital-to-Analog Coverter**
  Savoj, J., Abbasfar, A., Amirkhany, A., Garlepp, B., Jeeradit, M.
  2007
- **A 14mW 6.25Gb/s Transceiver in 90nm CMOS for Serial Chip-to-Chip Communications**
  Palmer, R., Poulton, J., Dally, W., J., Eyles, J., Fuller, A., M., Greer, T., Horowitz, M. A.
  2007
- **Synthetic aperture focusing using dense camera arrays** *Workshop on Advanced 3D Imaging for Safety and Security held in Conjunction with the International Conference on Computer Vision and Pattern Recognition*
  Vaish, V., Garg, G., Talvala, E., Antunez, E., Wilburn, B., Horowitz, M., Levoy, M.
  SPRINGER.2007: 159-?
- **A new technique for characterization of digital-to-analog converters in high-speed systems** *Design, Automation and Test in Europe Conference and Exhibition (DATE 07)*
  Savoj, J., Abbasfar, A., Amirkhany, A., Garlepp, B. W., Horowitz, M. A.
  IEEE.2007: 433–438
- **A 24Gb/s software programmable multi-channel transmitter** *20th Symposium on VLSI Circuits*
  Amirkhany, A., Abbasfar, A., Savoj, J., Jeeradit, M., Garlepp, B., Stoianovic, V., Horowitz, M.
  JAPAN SOCIETY APPLIED PHYSICS.2007: 38–39
- **Comparing Memory Systems for Chip Multiprocessors** *34th Annual International Symposium on Computer Architecture*
  Leverich, J., Arakida, H., Solomatnikov, A., Firoozshahian, A., Horowitz, M., Kozyrakis, C.

ASSOC COMPUTING MACHINERY.2007: 358–368

- **Noise analysis of LSO-PSAPD PET detector front-end multiplexing circuits** *IEEE Nuclear Science Symposium/Medical Imaging Conference*
  Lau, F. W., Olcott, P. D., Horowitz, M. A., Peng, H., Levin, C. S.
  IEEE.2007: 3212–3219
- **Practical limits of multi-tone signaling over high-speed backplane electrical links** *IEEE International Conference on Communications (ICC 2007)*
  Amirkhany, A., Abbasfar, A., Stojanovic, V., Horowitz, M. A.
  IEEE.2007: 2693–2698
- **Time-variant characterization and compensation of wideband circuits** *IEEE Custom Integrated Circuits Conference*
  Amirkhany, A., Abbasfar, A., Savoj, J., Horowitz, M. A.
  IEEE.2007: 487–490
- **Robust energy-efficient adder topologies** *18th IEEE Symposium on Computer Arithmetic*
  Patil, D., Azizi, O., Horowitz, M., Ho, R., Ananthraman, R.
  IEEE COMPUTER SOC.2007: 16–25
- **Measurement of supply pin current distributions in integrated circuit packages** *16th IEEE Topical Meeting on Electrical Performance of Electronic Packaging*
  Weaver, J. A., Horowitz, M. A.
  IEEE.2007: 7–10
- **Light field microscopy** *ACM TRANSACTIONS ON GRAPHICS*
  Levoy, M., Ng, R., Adams, A., Footer, M., Horowitz, M.
  2006; 25 (3): 924-934
- **Replica compensated linear regulators for supply-regulated phase-locked loops** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Alon, E., Kim, J., Pamarti, S., Chang, K., Horowitz, M.
  2006; 41 (2): 413-424
- **Analog Multi-Tone Signaling for High-Speed Backplane Electrical Links** *IEEE Global Telecommunications Conference (GLOBECOM 06)*
  Amirkhany, A., Abbasfar, A., Stojanovic, V., Horowitz, M. A.
  IEEE.2006
- **High-speed transmitters in 90nm CMOS for high-density optical interconnects** *32nd European Solid-State Circuits Conference*
  Palermo, S., Horowitz, M.
  IEEE.2006: 508–511
- **The implementation of a 2-core, multi-threaded Itanium family processor** *IEEE International Solid-State Circuits Conference (ISSCC 2005)*
  Naffziger, S., Stackhouse, B., Grutkowski, T., Josephson, D., Desai, J., Alon, E., Horowitz, M.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2006: 197–209
- **Measurement of via currents in printed circuit boards using inductive loops** *15th IEEE Topical Meeting on Electrical Performance of Electronic Packaging*
  Weaver, J. A., Horowitz, M. A.
  IEEE.2006: 37–40
- **A heuristic method for statistical digital circuit sizing** *4th Conference on Design and Process Integration for Microelectronic Manufacturing*
  Boyd, S., Kim, S., Patil, D., Horowitz, M.
  SPIE-INT SOC OPTICAL ENGINEERING.2006
- **Compensation for multimode fiber dispersion by adaptive optics** *OPTICS LETTERS*
  Shen, X. L., Kahn, J. M., Horowitz, M. A.
  2005; 30 (22): 2985-2987
- **Digital circuit optimization via geometric programming** *OPERATIONS RESEARCH*
  Boyd, S. P., Kim, S. J., Patil, D. D., Horowitz, M. A.
  2005; 53 (6): 899-932
- **False coupling exploration in timing analysis** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Tseng, K., Horowitz, M.

2005; 24 (11): 1795-1805

- **Dual photography** *ACM SIGGRAPH 2005 Conference*
  Sen, P., Chen, B., Garg, G., Marschner, S. R., Horowitz, M., Levoy, M., Lensch, H. P.
  ASSOC COMPUTING MACHINERY.2005: 745–55
- **High performance imaging using large camera arrays** *ACM SIGGRAPH 2005 Conference*
  Wilburn, B., Joshi, N., Vaish, V., Talvala, E. V., Antunez, E., Barth, A., Adams, A., Horowitz, M., Levoy, M.
  ASSOC COMPUTING MACHINERY.2005: 765–76
- **On task mapping optimization for parallel decoding of low-density parity-check codes on message-passing architectures** *PARALLEL COMPUTING*
  Al-Rawi, G., Cioffi, J., Horowitz, M.
  2005; 31 (5): 462-490
- **A 20-Gb/s 0.13-mu m CMOS serial link transmitter using an LC-PLL to directly drive the output multiplexer** *Symposium on VLSI Circuits*
  Chiang, P., Dally, W. J., Lee, M. J., Senthinathan, R., Oh, Y., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2005: 1004–11
- **Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery** *Symposium on VLSI Circuits*
  Stojanovic, V., Ho, A., Garlepp, B. W., Chen, F., Wei, J., Tsang, G., Alon, E., Kollipara, R. T., Werner, C. W., Zerbe, J. L., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2005: 1012–26
- **Circuits and techniques for high-resolution measurement of on-chip power supply noise** *Symposium on VLSI Circuits*
  Alon, E., Stojanovic, V., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2005: 820–28
- **Architecture and circuit techniques for a 1.1-GHz 16-kb reconfigurable memory in 0.18-mu m CMOS** *IEEE International Solid-State Circuits Conference*
  Mai, K., Ho, R., Alon, E., Liu, D., Kim, Y., Patil, D., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2005: 261–75
- **Clocking and circuit design for a parallel I/O on a first-generation CELL processor**
  Chang, K., Pamarti, S., Kaviani, K., Alon, E., Xudong, S., Chin, T., J., Horowitz, M. A.
  2005
- **A new method for design of robust digital circuits.**
  Patil, D., Yun, S., Kim, S., J, Cheung, A., Horowitz, M., Boyd, S.
  2005
- **Opportunities for optics in integrated circuits applications. Solid-State Circuits Conference**
  Miller, D., A. B., Bhatnagar, A., Palermo, S., Emami-Neyestanak, A., Horowitz, M., A.
  2005
- **High-speed videography using a dense camera array** *26th International Congress on High-Speed Photography and Photonics*
  Wilburn, B., Joshi, N., Vaish, V., Levoy, M., Horowitz, M.
  SPIE-INT SOC OPTICAL ENGINEERING.2005: 913–920
- **A new method for design of robust digital circuits** *6th International Symposium on Quality Electronic Design*
  Patil, D., Yun, S. H., Kim, S. J., Cheung, A., Horowitz, M., Boyd, S.
  IEEE COMPUTER SOC.2005: 676–681
- **Scaling, power, and the future of CMOS** *IEEE International Electron Devices Meeting*
  Horowitz, M., Alon, E., Patil, D., Naffziger, S., Kumar, R., Bernstein, K.
  IEEE.2005: 11–17
- **Scalable circuits for supply noise measurement** *31st European Solid-State Circuits Conference*
  Abramzon, V., Alon, E., Nezamfar, B., Horowitz, M.
  IEEE.2005: 463–466
- **Synthetic aperture confocal imaging** *Annual Symposium of the ACM SIGGRAPH*
  Levoy, M., Chen, B., Vaish, V., Horowitz, M., McDowall, I., Bolas, M.

ASSOC COMPUTING MACHINERY.2004: 825–34

- **Methods for true energy-performance optimization** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Markovic, D., Stojanovic, V., Nikolic, B., Horowitz, M. A., Brodersen, R. W.
  2004; 39 (8): 1282-1293

- **The stream virtual machine** *13th International Conference on Parallel Architecture and Compilation Techniques*
  Labonte, F., Mattson, P., Thies, W., Buck, I., Kozyrakis, C., Horowitz, M.
  IEEE COMPUTER SOC.2004: 267–277

- **Adaptive equalization and data recovery in a dual-mode (PAM2/4) serial link transceiver** *Symposium on VLSI Circuits*
  Stojanovic, V., Ho, A., Garlepp, B., Chen, F., Wei, J., Alon, E., Werner, C., Zerbe, J., Horowitz, M. A.
  IEEE.2004: 348–351

- **Common-mode backchannel signaling system for differential high-speed links** *Symposium on VLSI Circuits*
  Ho, A., Stojanovic, V., Chen, F., Werner, C., Tsang, G., Alon, E., Kollipara, R., Zerbe, J., Horowitz, M. A.
  IEEE.2004: 352–355

- **Burst mode packet receiver using a second order DLL** *Symposium on VLSI Circuits*
  LEE, H., YUE, C. H., Palermo, S., Mai, K. W., Horowitz, M.
  IEEE.2004: 264–267

- **Circuits and techniques for high-resolution measurement of on-chip power supply noise**
  Alon, E., Stojanovic, V., Horowitz, M.
  2004

- **Adaptive equalization and data recovery in a dual-mode (PAM2/4) serial link transceiver**
  Stojanovic, V., Ho, A., Garlepp, B., Chen, F., Wei, J., Alon, E., Horowitz, M. A.
  2004

- **Equalization of modal dispersion in multimode fiber using spatial light modulators** *IEEE Global Telecommunications Conference (GLOBECOM 04)*
  Alon, E., Stojanovic, V., Kahn, J. M., Boyd, S., Horowitz, M.
  IEEE.2004: 1023–1029

- **20Gb/s 0.13 mu m CMOS serial link transmitter using an LC-PLL to directly drive the output multiplexer**
  Chiang, P., Dally, W., J., Lee, M., J. E., Senthinathan, R., Yangjin, O., Horowitz, M.
  2004

- **Burst mode packet receiver using a second order DLL**
  Lee, H., C., Yue, C., H., Palermo, S., Mai, K., W., Horowitz, M.
  2004

- **Common-mode backchannel signaling system for differential high-speed links**
  Ho, A., Stojanovic, V., Chen, F., Werner, C., Tsang, G., Alon, E., Horowitz, M. A.
  2004

- **Optimal linear precoding with theoretical and practical data rates in high-speed serial-link backplane communication** *IEEE International Conference on Communications (ICC 2004)*
  Stojanovic, V., Amirkhany, A., Horowitz, M. A.
  IEEE.2004: 2799–2806

- **Multi-tone signaling for high-speed backplane electrical links** *IEEE Global Telecommunications Conference (GLOBECOM 04)*
  Amirkhany, A., Stojanovic, V., Horowitz, M. A.
  IEEE.2004: 1111–1117

- **CMOS transceiver with baud rate clock recovery for optical interconnects** *Symposium on VLSI Circuits*
  Emami-Neyestanak, A., Palermo, S., Lee, H. C., Horowitz, M.
  IEEE.2004: 410–413

- **High-speed videography using a dense camera array** *Conference on Computer Vision and Pattern Recognition*
  Wilburn, B., Joshi, N., Vaish, V., Levoy, M., Horowitz, M.

IEEE COMPUTER SOC.2004: 294–301

- **Architecture and circuit techniques for a reconfigurable memory block** *IEEE International Solid-State Circuits Conference*
  Mai, K., Ho, R., Alon, E., Liu, D., Kim, Y., Patil, D., Horowitz, M.
  IEEE.2004: 500–501

- **How scaling will change processor architecture** *IEEE International Solid-State Circuits Conference*
  Horowitz, M., Daily, W.
  IEEE.2004: 132–133

- **Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplane transceiver cell** *IEEE International Solid-State Circuits Conference*
  Zerbe, J. L., Werner, C. W., Stojanovic, V., Chen, F., Wei, J., Tsang, G., Kim, D., Stonecypher, W. F., Ho, A., Thrush, T. P., Kollipara, R. T., Horowitz, M. A., Donnelly, et al
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2003: 2121–30

- **A 10-GHz global clock distribution using coupled standing-wave oscillators** *IEEE International Solid-State Circuits Conference*
  O'Mahony, F., Yue, C. P., Horowitz, M. A., Wong, S. S.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2003: 1813–20

- **Design of CMOS adaptive-bandwidth PLL/DLLs: A general approach** *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II-EXPRESS BRIEFS*
  Kim, J., Horowitz, M. A., Wei, G. Y.
  2003; 50 (11): 860-869

- **Scaling Internet routers using optics** *SIGCOMM 2003 Conference*
  Keslassy, I., Chuang, S. T., Yu, K., Miller, D., Horowitz, M., Solgaard, O., McKeown, N.
  ASSOC COMPUTING MACHINERY.2003: 189–200

- **Efficient on-chip global interconnects** *Symposium on VLSI Circuits*
  Ho, R., Mai, K., Horowitz, M.
  JAPAN SOCIETY APPLIED PHYSICS.2003: 271–274

- **Implementing an untrusted operating system on trusted hardware.** *Operating Systems Review*
  Lie, D., Thekkath, C. A., Horowitz, M.
  2003; 37 (5): 178-92

- **A framework for designing reusable analog circuits**
  Liu, D., Sidiropoulos, S., Horowitz, M.
  2003

- **Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplane transceiver cell.** *IEEE Journal of Solid-State Circuits*
  Zerbe, J., L., Werner, C., W., Stojanovic, V., Chen, F., Wei, J., Tsang, G., Horowitz, M. A.
  2003; 38 (12): 2121 - 2130

- **Design of CMOS adaptive-bandwidth PLL/DLLs: a general approach. Circuits and Systems II: Analog and Digital Signal Processing** *IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on]*
  Kim, J., Horowitz, M., A., Wei, G.
  2003; 50 (11): 860-869

- **A 10-GHz global clock distribution using coupled standing-wave oscillators Solid-State Circuits** *IEEE Journal of*
  O'Mahony, F., Yue, C., P., Horowitz, M., A., Wong, S., S.
  2003; 38 (11): 1813-1820

- **Modeling and analysis of high-speed links**
  Stojanovic, V., Horowitz, M.
  2003

- **A 0.4-4-Gb/s CMOS quad transceiver cell using on-chip regulated dual-loop PLLs.** *IEEE Journal of Solid-State Circuits*
  Chang, K.-Y., K., Wei, J., Huang, C., Li, S., Donnelly, K., Horowitz, M.
  2003; 38 (5): 747-54

- **Specifying and verifying hardware for tamper-resistant software** *2003 IEEE Symposium on Security and Privacy*

Lie, D., Mitchell, J., Thekkath, C. A., Horowitz, M.
IEEE COMPUTER SOC.2003: 166–177

- **10GHz clock distribution using coupled standing-wave oscillators** *IEEE International Solid-State Circuits Conference*
  O'Mahony, F., Yue, C. P., Horowitz, M., Wong, S. S.
  IEEE.2003: 428-?
- **Design of a 10GHz clock distribution network using coupled standing-wave oscillators** *40th Design Automation Conference*
  O'Mahony, F., Yue, C. P., Horowitz, M. A., Wong, S. S.
  ASSOC COMPUTING MACHINERY.2003: 682–687
- **Managing wire scaling: A circuit perspective** *6th Annual International Interconnect Technology Conference*
  Ho, R., Mai, K., Horowitz, M.
  IEEE.2003: 177–179
- **Adaptive supply serial links with sub-I-V operation and per-pin clock recovery** *IEEE International Solid State Circuits Conference*
  Kim, J., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2002: 1403–13
- **High-frequency characterization of on-chip digital interconnects** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Kleveland, B., Qi, X. N., Madden, L., Furusawa, T., DUTTON, R. W., Horowitz, M. A., Wong, S. S.
  2002; 37 (6): 716-725
- **An efficient digital sliding controller for adaptive power-supply regulation** *Symposium on VLSI Circuits*
  Kim, J., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2002: 639–47
- **1.6 Gb/s, 3 mW CMOS receiver for optical communication**
  Emami-Neyestanak, A., Liu, D., Keeler, G., Helman, N., Horowitz, M., A.
  2002
- **Transmit pre-emphasis for high-speed time-division-multiplexed serial-link transceiver**
  Stojanovic, V., Ginis, G., Horowitz, M., A.
  2002
- **Methods for true power minimization**
  Brodersen, R., W., Horowitz, M., A., Markovic, D., Nikolic, B., Stojanovic, V.
  2002
- **Energy-delay tradeoffs in combinational logic using gate sizing and supply voltage optimization. ESSCIRC 2002**
  Stojanovic, V., Markovic, D., Nikolic, B., Horowitz, M., A., Brodersen, R., W.
  2002
- **Power Aware Design Methodologies.**
  Pedram, M.
  2002
- **A serial-link transceiver based on 8-GSamples/s A/D and D/A converters in 0.25-mu m CMOS** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Yang, C. K., Stojanovic, V., Modjtahedi, S., Horowitz, M. A., Ellersick, W. F.
  2001; 36 (11): 1684-1692
- **Fast low-power decoders for RAMs** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Amrutur, B. S., Horowitz, M. A.
  2001; 36 (10): 1506-1515
- **The future of wires** *PROCEEDINGS OF THE IEEE*
  Ho, R., Mai, K. W., Horowitz, M. A.
  2001; 89 (4): 490-504
- **Light field video camera**
  Wilburn, B., S., Smulski, M., Lee, H., K., Horowitz, M., A.

2001

- **Using texture mapping with mipmapping to render a VLSI layout**
  Solomon, J., Horowitz, M.
  2001
- **Sampling-rate optimization of an interleaved-sampling front-end. ISCAS 2001**
  H., M., O., Johansson
  2001
- **Optimizing iterative decoding of low-density parity check codes on programmable pipelined parallel architectures**
  Al-Rawi, G., Cioffi, J., Motwani, R., Horowitz, M.
  2001
- **A serial-link transceiver based on 8 GSample/s A/D and D/A converters in 0.25 mu m CMOS**
  Ellersick, W., Yang, C., K. K., Stojanovic, V., Modjtahedi, S., Horowitz, M., A.
  2001
- **High-Speed Electrical Signaling** *in Design of High-Performance Microprocessor Circuits*
  Horowitz, M., A.
  2001
- **Optimizing the mapping of low-density parity check codes on parallel decoding architectures**
  Al-Rawi, G., Cioffi, J., Horowitz, M.
  2001
- **Architectural support for copy and tamper resistant software** *9th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS_IX)*
  Lie, D., Thekkath, C., Mitchell, M., Lincoln, P., Boneh, D., Mitchell, J., Horowitz, M.
  ASSOC COMPUTING MACHINERY.2000: 168–77
- **FLASH vs. (Simulated) FLASH: Closing the simulation loop** *9th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS_IX)*
  Gibson, J., Kunz, R., Ofelt, D., Horowitz, M., Hennessy, J., Heinrich, M.
  ASSOC COMPUTING MACHINERY.2000: 49–58
- **A 2.4 gb/s/pin simultaneous bidirectional parallel link with per-pin skew compensation** *International Solid-State Circuits Conference*
  Yeung, E., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2000: 1619–28
- **A variable-frequency parallel I/O interface with adaptive power-supply regulation** *International Solid-State Circuits Conference*
  Wei, G. Y., Kim, J., Liu, D., Sidiropoulos, S., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2000: 1600–1610
- **A 0.3-mu m CMOS 8-Gb/s 4-PAM serial link transceiver** *Symposium on VLSI Circuits*
  Farjad-Rad, R., Yang, C. K., Horowitz, M. A., Lee, T. H.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.2000: 757–64
- **Speed and power scaling of SRAM's** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Amrutur, B. S., Horowitz, M. A.
  2000; 35 (2): 175-185
- **M. FLASH vs. (simulated) FLASH: closing the simulation loop** *Operating Systems Review*
  Gibson, J., Kunz, R., Ofelt, D., Horowitz, M., Hennessy, J., Heinrich, M., FLASH
  2000; 34 (5): 49-58
- **Adaptive bandwidth DLLs and PLLs using regulated supply CMOS buffers**
  Sidiropoulos, S., Liu, D., Kim, J., Wei, G., Horowitz, M.
  2000
- **Smart Memories: a modular reconfigurable architecture**

Mai, K., Paaske, T., Jayasena, N., Ho, R., Dally, W., J., Horowitz, M.
2000

- **An eight channel 35 GSample/s CMOS timing analyzer**
  Weinlader, D., Ron, H., Yang, C. K., Horowitz, M.
  2000
- **A 2.4 Gb/s/pin simultaneous bidirectional parallel link with per pin skew compensation**
  Yeung, E., Horowitz, M.
  2000
- **A variable-frequency parallel I/O interface with adaptive power-supply regulation.** *IEEE Journal of Solid-State Circuits*
  Wei, G., Kim, J., Liu, D., Sidiropoulos, S., Horowitz, M., A.
  2000; 35 (11): 1600-10
- **64 Mbit mesochronous hybrid wave pipelined multibank DRAM macro** *Intelligent Memory Systems. Second International Workshop, IMS 2000. Revised Papers, Cambridge, MA, USA.*
  Ogawa, J., Horowitz, M., A.
  2000
- **Timing analysis including clock skew** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Harris, D., Horowitz, M., Liu, D.
  1999; 18 (11): 1608-1618
- **A 0.4-mu m CMOS 10-Gb/s 4-PAM pre-emphasis serial link transmitter** *Symposium on VLSI Circuits*
  Farjad-Rad, R., Yang, C. K., Horowitz, M. A., Lee, T. H.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.1999: 580–85
- **A portable digital DLL for high-speed CMOS interface circuits** *Symposium on VLSI Circuits*
  Garlepp, B. W., Donnelly, K. S., Kim, J., Chau, P. S., Zerbe, J. L., Huang, C., Tran, C. V., Portmann, C. L., Stark, D., Chan, Y. F., Lee, T. H., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.1999: 632–44
- **A fully digital, energy-efficient, adaptive power-supply regulator** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Wei, G. Y., Horowitz, M.
  1999; 34 (4): 520-528
- **Using Partitioning to Help Convergence in the Standard-Cell Design Automation Methodology**
  Kapadia, H., Horowitz, M.
  1999
- **A 50 Gb/s 32*32 CMOS crossbar chip using asymmetric serial links**
  Chang, K. K., Chuang, S., McKeown, N., Horowitz, M.
  1999
- **A 0.3- mu m CMOS 8-Gb/s 4-PAM serial link transceiver**
  Farjad-Rad, R., Yang, C. K., Horowitz, M., Lee, T.
  1999
- **Using partitioning to help convergence in the standard-cell design automation methodology**
  Kapadia, H., Horowitz, M.
  1999
- **Scaling implications for CAD**
  Ho, R., Mai, K., Horowitz, M.
  1999
- **Improving Coverage Analysis and Test Generation for Large Designs**
  Bergmann, J., Horowitz, M.
  1999

- **GAD: A 12-GS/s CMOS 4-bit A/D converter for an equalized multi-level link**
  Ellersick, W., Yang, C. K., Horowitz, M., Dally, W.
  1999
- **Vex - A CAD Toolbox**
  Bergmann, J., P., Horowitz, M., A.
  1999
- **Low-power dividerless frequency synthesis using aperture phase detection** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Shahani, A. R., Shaeffer, D. K., Mohan, S. S., Samavati, H., Rategh, H. R., Hershenson, M. D., Xu, M., Yue, C. P., Eddleman, D. J., Horowitz, M. A., Lee, T. N.
  1998; 33 (12): 2232-2239
- **Low-power SRAM design using half-swing pulse-mode techniques** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Mai, K. W., Mori, T., Amrutur, B. S., Ho, R., Wilburn, B., Horowitz, M. A., Fukushi, I., Izawa, T., Mitarai, S.
  1998; 33 (11): 1659-1671
- **A replica technique for wordline and sense control in low-power SRAM's** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Amrutur, B. S., Horowitz, M. A.
  1998; 33 (8): 1208-1219
- **A 0.5-mu m CMOS 4.0-Gbit/s serial link transceiver with data recovery using oversampling** *1997 Symposium on VLSI Circuits*
  Yang, C. K., Farjad-Rad, R., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.1998: 713–22
- **Informing memory operations: Memory performance feedback mechanisms and their applications** *ACM TRANSACTIONS ON COMPUTER SYSTEMS*
  Horowitz, M., Martonosi, M., Mowry, T. C., Smith, M. D.
  1998; 16 (2): 170-205
- **High-speed electrical signaling: Overview and limitations** *IEEE MICRO*
  Horowitz, M., Yang, C. K., Sidiropoulos, S.
  1998; 18 (1): 12-24
- **A 2Gb/s Asymmetric Serial Link for High-bandwidth Packet Switches**
  Chang, K., K.-Y, Ellersick, W., Chuang, T., S., Sidiropoulos, S., Horowitz, M., McKeown, N.
  1998
- **Approximate reachability with BDDs using overlapping projections** *35th Design Automation Conference*
  Govindaraju, S. G., Dill, D. L., Hu, A. J., Horowitz, M. A.
  ASSOC COMPUTING MACHINERY.1998: 451–456
- **Applications of On-Chip Samplers for Test and Measurement of Integrated Circuits**
  Ho, R., Amrutur, B., Mai, K., Wilburn, B., Mori
  1998
- **A 0.4-µm CMOS 10-Gb/s 4-PAM Pre-Emphasis Serial Link Transmitter**
  Farjad-Rad, R., Yang, C-K, K., Horowitz, M.
  1998
- **A semidigital dual delay-locked loop** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Sidiropoulos, S., Horowitz, M. A.
  1997; 32 (11): 1683-1692
- **Skew-tolerant domino circuits** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Harris, D., Horowitz, M. A.
  1997; 32 (11): 1702-1711
- **Circuit techniques for 1.5-V power supply flash memory** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Otsuka, N., Horowitz, M. A.
  1997; 32 (8): 1217-1230

- **Supply and threshold voltage scaling for low power CMOS** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  GONZALEZ, R., Gordon, B. M., Horowitz, M. A.
  1997; 32 (8): 1210-1216
- **Optimization of hybrid JJ/CMOS memory operating temperatures** *1996 Applied Superconductivity Conference*
  Gupta, D., Amrutur, B., Terzioglu, E., Ghoshal, U., Beasley, M. R., Horowitz, M.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.1997: 3307–10
- **A 700-Mb/s/pin CMOS signaling interface wing current integrating receivers** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Sidiropoulos, S., Horowitz, M.
  1997; 32 (5): 681-690
- **Hardware/software co-design of the Stanford FLASH multiprocessor** *PROCEEDINGS OF THE IEEE*
  Heinrich, M., Ofelt, D., Horowitz, M. A., Hennessy, J.
  1997; 85 (3): 455-466
- **Skew-tolerant domino circuits** *1997 IEEE International Solid-State Circuits Conference*
  Harris, D., Horowitz, M. A.
  I E E E.1997: 422–423
- **Hardware fault containment in scalable shared-memory multiprocessors** *24th Annual International Symposium on Computer Architecture*
  Teodosiu, D., Baxter, J., Govil, K., Chapin, J., Rosenblum, M., Horowitz, M.
  ASSOC COMPUTING MACHINERY.1997: 73–84
- **A 0.6u CMOS 4.0Gbps Transceiver with Data Recovery using Oversampling**
  Yang, C., K, Farjad-Rad, R., Horowitz, M.
  1997
- **An Equalization Scheme for 10Gb/s 4-PAM Signaling over Long Cables**
  Farjad-Rad, K., Yu, Yang, C., K., Ellersick, W., Horowitz, M., Lee, T., H.
  1997
- **SRT Division Architectures and Implementations**
  Harris, D., L., Oberman, S., F., Horowitz, M., A.
  1997
- **A 0.6 mu m CMOS 4Gb/s transceiver with data recovery using oversampling** *1997 Symposium on VLSI Circuits*
  Yang, C. K., FarjadRad, R., Horowitz, M.
  JAPAN SOCIETY APPLIED PHYSICS.1997: 71–72
- **A semi-digital DLL with unlimited phase shift capability and 0.08-400MHz operating range** *1997 IEEE International Solid-State Circuits Conference*
  Sidiropoulos, S., Horowitz, M.
  I E E E.1997: 332–333
- **Tiny Tera: A packet switch core** *4th Annual Hot Interconnects Symposium*
  McKeown, N., IZZARD, M., Mekkittikul, A., Ellersick, W., Horowitz, M.
  IEEE COMPUTER SOC.1997: 26–33
- **A 0.8-mu m CMOS 2.5 Gb/s oversampling receiver and transmitter for serial links** *1996 International Solid-State Circuits Conference (ISSCC)*
  Yang, C. K., Horowitz, M. A.
  IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC.1996: 2015–23
- **Energy dissipation in general purpose microprocessors** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  GONZALEZ, R., Horowitz, M.
  1996; 31 (9): 1277-1284
- **A 0.8 mu m CMOS 2.5Gb/s oversampled receiver for serial links** *1996 IEEE International Solid-State Circuits Conference*
  Yang, C. K., Horowitz, M. A.
  I E E E.1996: 200–201

- **Validation Coverage Analysis for Complex Digital Designs**
  Ho, R., C., Horowitz, M., A.
  1996

- **Informing Memory Operations: Providing Memory Performance Feedback in Modern Processors**
  Horowitz, M., Martonosi, M., Mowry, T., C., Smith, M., D.
  1996

- **A 50% Noise Reduction Interface Using Low-Weight Coding**
  Nakamura, K., Horowitz, M., A.
  1996

- **Informing memory operations: Providing memory performance feedback in modem processors** *23rd Annual International Symposium on Computer Architecture*
  Horowitz, M., Martonosi, M., Mowry, T. C., Smith, M. D.
  ASSOC COMPUTING MACHINERY.1996: 260–270

- **A 700 Mbps/pin CMOS signalling interface using current integrating receivers** *1996 Symposium on VLSI Circuits*
  Sidiropoulos, S., Horowitz, M.
  I E E E.1996: 142–143

- **A low power switching power supply for self-clocked systems** *1996 International Symposium on Low Power Electronics and Design (1996 ISLPED)*
  Wei, G. Y., Horowitz, M.
  I E E E.1996: 313–317

- **Regenerative feedback repeaters for programmable interconnections** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Dobbelaere, I., Horowitz, M., Elgamal, A.
  1995; 30 (11): 1246-1253

- **REGENERATIVE FEEDBACK REPEATERS FOR PROGRAMMABLE INTERCONNECTIONS** *1995 IEEE International Solid-State Circuits Conference*
  Dobbelaere, I., Horowitz, M., Elgamal, A.
  I E E E.1995: 116–117

- **Array-of-arrays Architecture for Parallel Floating Point Multiplication** *Advanced Research in VLSI*
  Dhanesha, H., Falakshahi, K., Horowitz, M.
  1995: 150-157

- **Clustered Voltage Scaling Technique for Low-Power Design**
  Usami, K., Horowitz, M.
  1995

- **Informing Loads: Enabling Software to Observe and React to Memory Behavior** *Stanford University, Technical Report*
  Horowitz, M., Martonosi, M., Mowry, T., C., Smith, M., D.
  1995: CSL-TR-95-673

- **Architecture validation for processors** *22nd Annual International Symposium on Computer Architecture*
  Ho, R. C., Yang, C. H., Horowitz, M. A., Dill, D. L.
  ASSOC COMPUTING MACHINERY.1995: 404–413

- **Current integrating receivers for high speed system interconnects** *IEEE 1995 Custom Integrated Circuits Conference*
  Sidiropoulos, S., Horowitz, M.
  I E E E.1995: 107–110

- **TIMING ANALYSIS FOR PIECEWISE-LINEAR RSIM** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Kao, R., Horowitz, M.
  1994; 13 (12): 1498-1512

- **THE PERFORMANCE IMPACT OF FLEXIBILITY IN THE STANFORD FLASH MULTIPROCESSOR** *6th International Conference on Architectural Support for Programming Languages and Operating Systems*

Heinrich, M., KUSKIN, J., Ofelt, D., Heinlein, J., Baxter, J., Singh, J. P., Simoni, R., Gharachorloo, K., NAKAHIRA, D., Horowitz, M., Gupta, A., Rosenblum, M., Hennessy, et al

ASSOC COMPUTING MACHINERY.1994: 274–85

- **INTERLEAVING - A MULTITHREADING TECHNIQUE TARGETING MULTIPROCESSORS AND WORKSTATIONS** *6th International Conference on Architectural Support for Programming Languages and Operating Systems*

  LAUDON, J., Gupta, A., Horowitz, M.

  ASSOC COMPUTING MACHINERY.1994: 308–18

- **SELF-TIMED LOGIC USING CURRENT-SENSING COMPLETION DETECTION (CSCD)** *JOURNAL OF VLSI SIGNAL PROCESSING*

  Dean, M. E., Dill, D. L., Horowitz, M.

  1994; 7 (1-2): 7-16

- **THE STANFORD FLASH MULTIPROCESSOR** *21st Annual International Symposium on Computer Architecture*

  KUSKIN, J., Ofelt, D., Heinrich, M., Heinlein, J., Simoni, R., Gharachorloo, K., Chapin, J., NAKAHIRA, D., Baxter, J., Horowitz, M., Gupta, A., Rosenblum, M., Hennessy, et al

  I E E E, COMPUTER SOC PRESS.1994: 302–313

- **Techniques to Reduce Power in Fast Wide Memories (CMOS SRAMS)**

  Amrutur, B., S., Horowitz, M.

  1994

- **Using Partitioning to Help Convergence in the Standard-cell Design Automation Methodology**

  Kapadia, H., Horowitz, M.

  1994

- **Techniques for Characterizing DRAMS with a 500 MHZ Interface**

  Gasbarro, J., A., Horowitz, M., A.

  1994

- **Low-Power Digital Design**

  Horowitz et al, M.

  1994

- **Evaluation of Charge Recovery Circuits and Adiabatic Switching for Low Power CMOS Design**

  Indermaur, T., Horowitz, M.

  1994

- **Architectural and Implementation Tradeoffs in the Design of Multiple-Context Processors** *Multithreaded Computer Architectures*

  Laudon, J., Gupta, A., Horowitz, M.

  Kluwer Academic Publishers.1994: 1

- **WHO WILL WIN THE WINDOWS NT SILICON SWEEPSTAKES** *1994 IEEE International Solid-State Circuits Conference*

  Horowitz, M., Slager, J., Heller, A., Tredennick, N., Riordan, T., Dobberpuhl, D., DHAM, V., MOTHERSOLE, D.

  I E E E.1994: 234–235

- **A CMOS 500-MBPS PIN SYNCHRONOUS POINT-TO-POINT LINK INTERFACE** *1994 Symposium on VLSI Circuits*

  Sidiropoulos, S., Yang, C. K., Horowitz, M.

  I E E E.1994: 43–44

- **PRECISE DELAY GENERATION USING COUPLED OSCILLATORS** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*

  Maneatis, J. G., Horowitz, M. A.

  1993; 28 (12): 1273-1282

- **THE DESIGN OF A HIGH-PERFORMANCE CACHE CONTROLLER - A CASE-STUDY IN ASYNCHRONOUS SYNTHESIS** *INTEGRATION-THE VLSI JOURNAL*

  Nowick, S. M., Dean, M. E., Dill, D. L., Horowitz, M.

  1993; 15 (3): 241-262

- **NONDESTRUCTIVE READOUT ARCHITECTURE FOR A KINETIC INDUCTANCE MEMORY CELL** *IEEE TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY*

Chen, G. J., Beasley, M. R., Horowitz, M., Rosenthal, P., Whiteley, S.
1993; 3 (1): 2702-2705

- **NONDESTRUCTIVE READOUT ARCHITECTURE FOR A KINETIC INDUCTANCE MEMORY CELL** *1992 Applied Superconductivity Conference*
  Chen, G. J., Beasley, M. R., Horowitz, M., Rosenthal, P., Whiteley, S.
  I E E E.1993: 2702–2705
- **Piecewise Linear Models for Rsim**
  Kao, R., Horowitz, M.
  1993
- **PLL Design for a 500 MB/s Interface**
  Horowitz et al, M.
  1993
- **Performance Analysis of a Kinetic Inductance Memory Array**
  Chen, G., J., Beasley, M., R., Horowitz, M.
  1993
- **EFFICIENT SUPERSCALAR PERFORMANCE THROUGH BOOSTING** *SIGPLAN NOTICES*
  Smith, M. D., Horowitz, M., Lam, M. S.
  1992; 27 (9): 248-259
- **CIRCUIT TECHNIQUES FOR LARGE CSEA SRAMS** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  WINGARD, D. E., Stark, D. C., Horowitz, M. A.
  1992; 27 (6): 908-919
- **THE STANFORD DASH MULTIPROCESSOR** *COMPUTER*
  Lenoski, D., LAUDON, J., Gharachorloo, K., Weber, W. D., Gupta, A., Hennessy, J., Horowitz, M., Lam, M. S.
  1992; 25 (3): 63-79
- **Circuit Techniques for Large CSEA SRAM's** *IEEE Journal of Solid-State Circuits*
  Wingard, D., E., Stark, D., C., Horowitz, M., A.
  1992; 27 (6): 908-919
- **A 500-Megabyte/s Data-Rate 4.5M DRAM**
  Kushiyama et al, N.
  1992
- **Clocking Strategies in High Performance Processors**
  Horowitz et al., M.
  1992
- **Architectural and Implementation Tradeoffs in the Design of Multiple-Context Processors**
  Laudon et al., J.
  1992
- **500 Mbyte/sec Data-Rate 512 Kbits*9 DRAM Using a Novel I/O Interface**
  Kushiyama et al., N.
  1992
- **A ZERO-OVERHEAD SELF-TIMED 160-NS 54-B CMOS DIVIDER** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Williams, T. E., Horowitz, M. A.
  1991; 26 (11): 1651-1661
- **Dynamic Pointer Allocation for Scalable Cache Coherence Directories**
  Simoni, R., Horowitz, M.
  1991
- **A 160NS 54BIT CMOS DIVISION IMPLEMENTATION USING SELF-TIMING AND SYMMETRICALLY OVERLAPPED SRT STAGES** *10TH IEEE SYMP ON COMPUTER ARITHMETIC*

Williams, T. E., Horowitz, M. A.
I E E E, COMPUTER SOC PRESS.1991: 210–217

- **Asymptotic Waveform Evaluation for Circuits With Redundant DC Equations** *Stanford University, Technical Report*
  Kao, R., Horowitz, M.
  1991: CSL-TR-91-478
- **A 160nS 54bit CMOS Division Implementation Using Self-Timing and Symmetrically Overlapped SRT Stages**
  Williams, T., E., Horowitz, M., A.
  1991
- **Efficient Moment-Based Timing Analysis for Variable Accuracy Switch Level Simulation** *Stanford University, Technical Report*
  Kao, R., Horowitz, M.
  1991: CSL-TR-91-468
- **Dynamic Pointer Allocation for Scalable Cache Coherence Directories** *Stanford University, Technical Report*
  Simoni, R., Horowitz, M.
  1991: CSL-TR-91-491
- **Modeling the Performance of Limited Pointers Directories for Cache Coherence**
  Simoni, R., Horowitz, M.
  1991
- **A 4-NS BICMOS TRANSLATION-LOOKASIDE BUFFER** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  TAMURA, L. R., Yang, T. S., WINGARD, D. E., Horowitz, M. A., Wooley, B. A.
  1990; 25 (5): 1093-1101
- **TECHNIQUES FOR CALCULATING CURRENTS AND VOLTAGES IN VLSI POWER-SUPPLY NETWORKS** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Stark, D., Horowitz, M.
  1990; 9 (2): 126-132
- **A Single-Chip, Functional Tester for VLSI Circuits**
  Gasbarro, J., Horowitz, M., A., Testarossa, M.
  1990
- **BOOSTING BEYOND STATIC SCHEDULING IN A SUPERSCALAR PROCESSOR** *17TH ANNUAL INTERNATIONAL SYMP ON COMPUTER ARCHITECTURE*
  Smith, M. D., Lam, M. S., Horowitz, M. A.
  I E E E, COMPUTER SOC PRESS.1990: 344–354
- **Boosting Beyond Static Scheduling in a Superscalar Processor** *Stanford University, Technical Report*
  Smith, M., D., Lam, M., S., Horowitz, M., A.
  1990: CSL-TR-90-434
- **Design of Scalable Shared-Memory Multiprocessors: the DASH Approach, Held: San Francisco, CA**
  Lenoski et al., D.
  1990
- **Boosting Beyond Static Scheduling in a Superscalar Processor**
  Horowitz, M., D.
  1990
- **BiCMOS Circuit Design**
  Horowitz et al., M.
  1990
- **A 3.5ns, 1 Watt, ECL Register File**
  Horowitz, M., Slamowitz, M., Rose, B., Johnson, M.
  1990

- **Limits on Multiple Instruction Issue** *Stanford University, Technical Report*
  Smith, M., D., Johnson, M., Horowitz, M., A.
  1990: CSL-TR-90-433
- **AN ANALYTICAL CACHE MODEL** *ACM TRANSACTIONS ON COMPUTER SYSTEMS*
  Agarwal, A., Horowitz, M., Hennessy, J.
  1989; 7 (2): 184-215
- **SPIM - A PIPELINED 64 X 64-BIT ITERATIVE MULTIPLIER** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Santoro, M. R., Horowitz, M. A.
  1989; 24 (2): 487-493
- **Design of the Stanford Dash Multiprocessor** *Stanford University, Technical Report*
  Lenoski, D., Laudon, J., Gharachorloo, K., Gupta, A., Hennessy, J., Horowitz, M.
  1989: CSL-TR-89-403
- **IRSIM: An Incremental MOS Switch-Level Simulator, IEEE/ACM**
  Salz, A., Horowitz, M.
  1989
- **Rounding Algorithms for IEEE Multipliers**
  Santoro, M., Bewick, G., Horowitz, M.
  1989
- **Characteristics of Performance-Optimal Multi-Level Cache Hierarchies**
  Przybylski, S., Horowitz, M., Hennessy, J.
  1989
- **A Single-Ended BiCMOS Sense Circuit for Digital Circuit**
  Rosseel, G., Horowitz, M., Cline, R., Dutton, R.
  1989
- **The MIPS-X RISC Microprocessor**
  Acken, J., Agarwal, A., Gulak, G., Horowitz, M., McFarling, S., Richardson, S.
  Kluwer Academic Publishers.1989
- **Integrated Pin Electronics for VLSI Functional Testers**
  Gasbarro, J., Horowitz, M.
  1989
- **CACHE PERFORMANCE OF OPERATING SYSTEM AND MULTIPROGRAMMING WORKLOADS** *ACM TRANSACTIONS ON COMPUTER SYSTEMS*
  Agarwal, A., Hennessy, J., Horowitz, M.
  1988; 6 (4): 393-431
- **A 4-NS 4K X 1-BIT 2-PORT BICMOS SRAM** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Yang, T. S., Horowitz, M. A., Wooley, B. A.
  1988; 23 (5): 1030-1040
- **SPECIAL ISSUE ON LOGIC AND MEMORY - FOREWORD** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Shah, A. H., Horowitz, M. A.
  1988; 23 (5): 1028-1029
- **Bisim: A Simulator for Custom ECL Circuits**
  Kao, R., Alverson, R., Horowitz, M., Stark, D.
  1988
- **Performance Tradeoffs in Cache Design, IEEE**
  Przybylski, S., Horowitz, M., Hennessy, J.
  1988

- **Scalable Directory Schemes for Cache Consistency**
  Agarwal, A., Simoni, R., Hennessy, J., Horowitz, M.
  1988
- **A 4nsec 4Kx1bit Two-Port BiCMOS SRAM**
  Yang, T. S., Horowitz, M., Wooley, B.
  1988
- **The Design and Testing of MIPS-X** *Advanced Research in VLSI, Cambridge, MA*
  Chow, P., Horowitz, M.
  MIT Press.1988: 95–114
- **Generalization in Digital Functions** *International Neural Network Society 1988 First Annual Meeting, Boston, MA, Neural Networks*
  Horowitz, M., Huyser et al, Karen, A.
  1988; 1 (1): 101
- **CHARGE-SHARING MODELS FOR SWITCH-LEVEL SIMULATION** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Chu, C. Y., Horowitz, M. A.
  1987; 6 (6): 1053-1061
- **MIPS-X - A 20-MIPS PEAK, 32-BIT MICROPROCESSOR WITH ON-CHIP CACHE** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Horowitz, M., Chow, P., Stark, D., SIMONI, R. T., SALZ, A., PRZYBYLSKI, S., Hennessy, J., Gulak, G., Agarwal, A., Acken, J. M.
  1987; 22 (5): 790-799
- **A SINGLE-CHIP LSI HIGH-SPEED FUNCTIONAL TESTER** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  MIYAMOTO, J. I., Horowitz, M. A.
  1987; 22 (5): 820-828
- **Architectural Tradeoffs in the Design of MIPS-X**
  Chow, P., Horowitz, M.
  1987
- **Toriodal Compaction of Symbolic Layouts for Regular Structures**
  Eichenberger, P., Horowitz, M.
  1987
- **On-Chip Instruction Caches for High Performance Processors**
  Horowitz, M., Agarwal et al, A.
  1987
- **A Static RAM as a Fault Model Evaluator**
  Acken, J., Horowitz, M.
  1987
- **A Self Timing SRT Division Chip** *Advanced Research in VLSI, Stanford, CA*
  Williams, T., E., Horowitz, M., Alverson, R., L., Yang, T., S.
  MIT Press.1987: 75–95
- **REDS: Resistance Extraction for Digital Stimulation, ACM/IEEE**
  Stark, D., Horowitz, M.
  1987
- **Generating Incremental VLSI Compaction Spacing Constraints, ACM/IEEE**
  Carpenter, C., Horowitz, M.
  1987
- **Active Substrate System Integration**
  Wooley, B., Horowitz, M., Pease, R., Yang, T.
  1987

- **An Overview of the MIPS-X-MP Project** *Stanford University, Technical Report*
  Hennessy, J., Horowitz, M.
  1986: CSL-TR-86-300
- **An Analytical Cache Model** *Stanford University, Technical Report*
  Agarwal, A., Horowitz, M., Hennessy, J.
  1986: CSL-TR-86-304
- **ATUM: A New Technique for Capturing Address Traces Using Microcode**
  Agarwal, A., Sites, R., Horowitz, M.
  1986
- **SRT Division Diagrams and Their Usage in Designing Custom Integrated Circuits for Division** *Stanford University, Technical Report*
  Williams, T., Horowitz, M.
  1986: CSL-TR-87-326
- **The MIPS-X Microprocessor** *WESCON 1985, San Francisco, CA*
  Horowitz, M., Chow, P.
  Published by Electronic Conventions Management, USA, Distributed by Western Periodicals Co, North Hollywood, CA.1985: 6. 1
- **An Automated Pressure Regulator** *Review of Scientific Instruments*
  Waxman, M., Davis, H., A., Horowitz, M., Everhart, B.
  1984; 55 (9): 1467-1470
- **A Low Cost Laser Interferometer System for Machine Tool Applications** *Precision Engineering*
  Dorsey, A., Hocken, R.
  1983; 5 (1): 29-31
- **Timing Models for MOS Pass Nets**
  Horowitz, M.
  1983
- **Resistance Extraction from Mask Layout Data** *IEEE Transactions on Computer-Aided Design*
  Horowitz, M., Dutton, R.
  1983; CAD-2 (3): 145-150
- **Timing Models for MOS Circuits** *Stanford University, Ph.D. Thesis, Dec. 1983. Also appears as Stanford University, Technical Report*
  Horowitz, M.
  1983: SEL-83-003
- **Signal Delay in RC Tree Networks** *IEEE Transactions on Computer-Aided Design*
  Rubinstein, J., Penfield, P., Horowitz, M.
  1983; CAD-2 (3): 202-211
- **A 14 BIT DUAL-RAMP DAC FOR DIGITAL-AUDIO SYSTEMS** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Mack, W. D., Horowitz, M., BLAUSCHILD, R. A.
  1982; 17 (6): 1118-1126
- **A 14 Bit Dual Ramp DAC for Digital Audio** *IEEE Journal of Solid-State Circuits, Shorter version in Proceedings of International Solid-State Circuits Conference (ISSCC), San Francisco, CA*
  Mack, W., Horowitz, M., Blauschild, R.
  1982; SC-17 (6): 86-87
- **A 14B PCM DAC** *ISSCC DIGEST OF TECHNICAL PAPERS*
  Mack, B., Horowitz, M., BLAUSCHILD, R.
  1982; 25: 86-?
- **MEASUREMENT OF SERIES COLLECTOR RESISTANCE IN BIPOLAR-TRANSISTORS** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Mack, W. D., Horowitz, M.
  1982; 17 (4): 767-773

- **Critical Anomaly in the Dielectric Constant of a Non-polar Pure Fluid** *Phy Rev Letters*
  Hocken, R., Horowitz, M., Greer, S.
  1976; 37 (15): 964-967
- **Why Design Must Change: Rethinking Digital Design** *Micro, IEEE*
  Shacham, O., Azizi, O., Wachs, M., Richardson, S., Horowitz, M.
  ; PP (99): 1-1
- **Analyzing CMOS Power Supply Networks Using Ariel, ACM/IEEE**
  Stark, D., Horowitz, M.
- **Measurement of Supply Pin Current Distributions in Integrated Circuit Packages**
  Weaver, James, A., Horowitz, Mark, A.
- **Nondestructive Readout Architecture for a Kinetic Inductance Memory Cell**
  Chen, G., J., Beasley, M., R., Rosenthal, P., R., Horowitz, M., Whiteley, S.
  1992, 1993
- **SPIM: A Pipelined 64 x 64 Bit Iterative Multiplier**
  Santoro, M., Horowitz, M.
  1989, 1988
- **Limits on Multiple Instruction Issue**
  Smith, M., Johnson, M., Horowitz, M.
  1989, 1990

PRESENTATIONS

- Hardware System Trends (March 1, 2023)