Bio

Jeff is a Ph.D. candidate at Stanford University in Electrical Engineering advised by Mark Horowitz. His research interests are in building hardware accelerators from software languages. Halide to Hardware is a project to use a data-parallel functional program formerly developed for CPU programs to produce hardware. Through the AHA hardware toolflow, these image processing and deep learning algorithms are mapped to a CGRA. Previously, Jeff received a B.S. in Electrical and Computer Engineering from Cornell University in 2015.

Publications

PUBLICATIONS

- **Interstellar: Using Halide’s Scheduling Language to Analyze DNN Accelerators**
  Yang, X., Gao, M., Liu, Q., Setter, J., Pu, J., Nayak, A., Bell, S., Cao, K., Ha, H., Raina, P., Kozyrakis, C., Horowitz, M., ACM
  ASSOC COMPUTING MACHINERY.2020: 369–83

- **Creating an Agile Hardware Design Flow**
  IEEE.2020

- **Programming Heterogeneous Systems from an Image Processing DSL** *ACM TRANSACTIONS ON ARCHITECTURE AND CODE OPTIMIZATION*
  Pu, J., Bell, S., Yang, X., Setter, J., Richardson, S., Ragan-Kelley, J., Horowitz, M.
  2017; 14 (3)