Stanford



Navid Anjum Aadit

Postdoctoral Scholar, Electrical Engineering

Bio

BIO

Navid Anjum Aadit is a postdoctoral scholar in Electrical Engineering at Stanford University, working with Prof. Subhasish Mitra on monolithic 3D CMOS +X integration and multi-chiplet systems for energy-efficient AI hardware, spanning architecture and chiplet design through tape-out, emulation-based verification, and post-silicon measurement.

He completed his PhD in Electrical and Computer Engineering at UC Santa Barbara in 2025 with Prof. Kerem Y. Camsari, where his work established probabilistic computing with p-bits as a practical hardware platform. He led the design of the first programmable probabilistic computer at the one-million p-bit scale, a distributed machine built from networked FPGAs, which was featured by IEEE Spectrum. His work spans combinatorial optimization, energy-based machine learning, and quantum simulation, and includes first-author papers in Nature Electronics and Nature Communications.

He is a recipient of the 2025 Misha Mahowald Prize for neuromorphic engineering, a 2023 Bell Labs Prize (Bronze), and the 2025 UCSB ECE Outstanding Dissertation Award.

HONORS AND AWARDS

- Bell Labs Prize, Bronze, Nokia Bell Labs (2023)
- Misha Mahowald Prize for Neuromorphic Engineering (OPUS team, UC Santa Barbara), Misha Mahowald Prize Committee (2025)
- UCSB ECE Outstanding Dissertation Award, Department of Electrical and Computer Engineering, University of California, Santa Barbara (2025)
- PhD Dissertation Fellowship, Graduate Division, University of California, Santa Barbara (2025)
- DTEI Fellowship, Division of Teaching Excellence and Innovation, University of California, Irvine (2020)
- NSF MRSEC Research Fellowship, University of California, Irvine (2020)

BOARDS, ADVISORY COMMITTEES, PROFESSIONAL ORGANIZATIONS

- Scientific Committee Member, International Workshop on Ising Machines (IISM) (2026 - 2026)
- Reviewer, Nature Scientific Reports; Communications Physics; PLOS ONE; Digital Discovery (2021 - present)
- Reviewer, IEEE journals: Journal on Exploratory Solid-State Computational Devices and Circuits (JXCDC); Transactions on Nanotechnology; Transactions on Computer-Aided Design of Integrated Circuits and Systems; Transactions on Affective Computing; Access (2021 - present)

PROFESSIONAL EDUCATION

- PhD, University of California, Santa Barbara , Electrical and Computer Engineering (2025)
- MS, University of California, Irvine , Electrical and Computer Engineering (2020)

- B.Sc., Bangladesh University of Engineering and Technology , Electrical and Electronic Engineering (2016)

STANFORD ADVISORS

- Subhasish Mitra, Postdoctoral Faculty Sponsor

LINKS

- Personal website: https://navidaadit.github.io
- Google Scholar: https://scholar.google.com/citations?user=KXA0nl4AAAAJ&hl=en
- LinkedIn: https://www.linkedin.com/in/navidanjumaadit

Research & Scholarship

RESEARCH INTERESTS

- Artificial intelligence (AI)

CURRENT RESEARCH AND SCHOLARLY INTERESTS

Navid Anjum Aadit builds computing hardware for problems that resist conventional acceleration: high-dimensional sampling, combinatorial search, and large AI models under hard energy budgets. His research spans the full stack these problems demand, from the Monte Carlo algorithms that solve them, through the architectures that execute them efficiently, down to the device physics that makes those architectures possible. Two commitments organize the work: that a computation should exploit the physics of its substrate rather than abstract away from it, and that memory and compute belong co-located rather than separated by a package boundary.

Monolithic 3D integration. At Stanford, working with Prof. Subhasish Mitra, Aadit works on monolithic 3D CMOS+X: silicon CMOS, carbon nanotube transistors, and resistive memory fabricated as one vertically integrated stack. Placing dense non-volatile memory immediately above compute reduces the off-chip traffic that dominates inference energy and changes how much of a model a single die can hold. He contributes across accelerator architecture and chiplet design, tape-out, emulation-based verification, bring-up, debug, and post-silicon characterization, including multi-chiplet systems engineered so that many physical dies behave as one logical device.

Probabilistic computing. A probabilistic bit, or p-bit, fluctuates between 0 and 1 with a tunable probability, and networks of p-bits sample from distributions rather than evaluating functions. Algorithmically, his work maps adaptive parallel tempering, discrete-time simulated quantum annealing, and non-equilibrium Monte Carlo onto massively parallel hardware, and develops the sparsification and higher-order embedding techniques that allow sparse hardware to represent densely connected problems without sacrificing solution quality. Architecturally, he has designed sparse Ising machines on CMOS and FPGAs, heterogeneous systems pairing CMOS with stochastic magnetic tunnel junctions, and the first programmable probabilistic computer at the million p-bit scale, distributed across networked chips. The applications extend well past optimization, to energy-based machine learning and the training of deep Boltzmann networks, to Bayesian inference, and to sampling the quantum states of many-body systems. This work has appeared in Nature Electronics, Nature Communications, Physical Review Applied, IEDM and the VLSI Symposium, and has been featured by IEEE Spectrum. It was recognized with the 2025 Misha Mahowald Prize for neuromorphic engineering and the 2025 UCSB ECE Outstanding Dissertation Award.

Convergence. Probabilistic machines have so far been built largely from FPGAs, which caps their density and energy efficiency. Dense stochastic memory, which monolithic 3D integration makes manufacturable, is a more compelling substrate, and the two research directions therefore converge. Aadit's program follows from that convergence: co-designing Monte Carlo algorithms, probabilistic architectures, and three-dimensionally integrated stochastic devices into accelerators for sampling and inference that no single layer of the stack reaches alone. The longer aim is hardware in which

probability is the computational primitive and vertical integration supplies the density to make it competitive with conventional machines on energy and cost, and with quantum annealers on time to solution for the problems both target.

LAB AFFILIATIONS

- Subhasish Mitra, Robust Systems Group (1/1/2026)

Publications

PUBLICATIONS

- **Pushing the boundary of quantum advantage in hard combinatorial optimization with probabilistic computers** *NATURE COMMUNICATIONS*
  Chowdhury, S., Aadit, N., Grimaldi, A., Raimondo, E., Raut, A., Lott, P., Mentink, J. H., Rams, M. M., Ricci-Tersenghi, F., Chiappini, M., Theogarajan, L. S., Srimani, T., Finocchio, et al
  2025; 16 (1): 9193

- **Scalable connectivity for Ising machines: Dense to sparse** *PHYSICAL REVIEW APPLIED*
  Sajeeb, M., Aadit, N., Chowdhury, S., Wu, T., Smith, C., Chinmay, D., Raut, A., Camsari, K. Y., Delacour, C., Srimani, T.
  2025; 24 (1)

- **All-to-all reconfigurability with sparse and higher-order Ising machines** *NATURE COMMUNICATIONS*
  Nikhar, S., Kannan, S., Aadit, N., Chowdhury, S., Camsari, K. Y.
  2024; 15 (1): 8977

- **Training deep Boltzmann networks with sparse Ising machines** *NATURE ELECTRONICS*
  Niazi, S., Chowdhury, S., Aadit, N., Mohseni, M., Qin, Y., Camsari, K. Y.
  2024; 7 (7)

- **CMOS plus stochastic nanomagnets enabling heterogeneous computers for probabilistic inference and learning** *NATURE COMMUNICATIONS*
  Singh, N., Kobayashi, K., Cao, Q., Selcuk, K., Hu, T., Niazi, S., Aadit, N., Kanai, S., Ohno, H., Fukami, S., Camsari, K. Y.
  2024; 15 (1): 2685

- **A Full-Stack View of Probabilistic Computing With p-Bits: Devices, Architectures, and Algorithms** *IEEE JOURNAL ON EXPLORATORY SOLID-STATE COMPUTATIONAL DEVICES AND CIRCUITS*
  Chowdhury, S., Grimaldi, A., Aadit, N., Niazi, S., Mohseni, M., Kanai, S., Ohno, H., Fukami, S., Theogarajan, L., Finocchio, G., Datta, S., Camsari, K. Y.
  2023; 9 (1): 1-11

- **Efficient Probabilistic Computing with Stochastic Perovskite Nickelates** *NANO LETTERS*
  Park, T., Selcuk, K., Zhang, H., Manna, S., Batra, R., Wang, Q., Yu, H., Aadit, N., Sankaranarayanan, S. S., Zhou, H., Camsari, K. Y., Ramanathan, S.
  2022: 8654-8661

- **Massively parallel probabilistic computing with sparse Ising machines** *NATURE ELECTRONICS*
  Aadit, N., Grimaldi, A., Carpentieri, M., Theogarajan, L., Martinis, J. M., Finocchio, G., Camsari, K. Y.
  2022; 5 (7): 460-468

- **Spintronics-compatible Approach to Solving Maximum-Satisfiability Problems with Probabilistic Computing, Invertible Logic, and Parallel Tempering** *PHYSICAL REVIEW APPLIED*
  Grimaldi, A., Sanchez-Tejerina, L., Aadit, N., Chiappini, S., Carpentieri, M., Camsari, K., Finocchio, G.
  2022; 17 (2)

- **Computing with Invertible Logic: Combinatorial Optimization with Probabilistic Bits**
  Aadit, N., Grimaldi, A., Carpentieri, M., Theogarajan, L., Finocchio, G., Camsari, K. Y., IEEE
  IEEE.2021

PRESENTATIONS

- CMOS plus stochastic MTJ: Heterogeneous probabilistic computers for optimization and sampling - Research Institute of Electrical Communication (RIEC), Tohoku University

- Probabilistic Computing on FPGAs: Extreme Scale Ising Machines with Distributed p-computers - Siemens Digital Industries Software
- Scaling Probabilistic Computers for Sustainable Computing - Semiconductor Research Corporation (SRC)
- Extreme Scale Ising Machines with Distributed p-computers - International Workshop on Ising Machines (IISM)
- Accelerating Adaptive Parallel Tempering with FPGA-based p-bits - VLSI Technology and Circuits Symposium
- Experimental evaluation of simulated quantum annealing with MTJ-augmented p-bits - IEEE International Electron Devices Meeting (IEDM)