Stanford



Young Suh Song

Ph.D. Student in Electrical Engineering, admitted Autumn 2024

Bio

BIO

Young Suh Song is a semiconductor researcher with a focus on electro-thermal co-design for advanced semiconductor devices and systems. His research interests include electro-thermal co-design for logic and memory applications, gate-all-around (GAA) nanosheet transistors, 2D semiconductors for logic applications, amorphous oxide semiconductor for memory applications, complementary field-effect transistor (CFET), nanostack transistors, backside power delivery network (BSPDN), and thermal management for next-generation computing systems.

He has authored and co-authored over 50 research papers in journals and conferences including Nature Nanotechnology, ACS Nano, IEEE Transactions on Electron Devices (IEEE TED), IEEE International Electron Devices Meeting (IEEE IEDM), IEEE Device Research Conference (IEEE DRC), IEEE International Reliability Physics Symposium (IEEE IRPS), and IEEE Electron Devices Technology & Manufacturing Conference (IEEE EDTM).

His academic contributions include editorial leadership for academic book projects with Springer and CRC Press, editorial contributions to Wiley publications, and trusted reviewer for ECS-IOP publications. He served on the technical committee for the IEEE International Conference on Circuits, Systems and Simulations (IEEE ICCSS) in 2022. He previously held a faculty appointment as an Assistant Professor in the Department of Computer Science at the Korea Military Academy. He has served as a guest speaker at universities including VIT-AP University and VIT-Chennai University (India) in 2022, NIT Delhi (India) in 2023, and ECE 290 Seminar at University of California Santa Cruz (United States) in 2026. He previously worked as a research scientist at IBM T. J. Watson Research Center, focusing on electro-thermal co-optimization in advanced CMOS nodes. His interdisciplinary work has been recognized with several honors, including 2 Top-Ranked Student Papers at IEEE IEDM (2025), the Outstanding Reviewer Award for Semiconductor Science and Technology (IOP Publishing, 2025), the Best Presentation Award at IEEE ICCSS (2022), and the Best Paper Award from IEIE (2020).

His research works can be found on the following website as well.

https://sites.google.com/view/yssong24

HONORS AND AWARDS

- Top-Ranked Student Paper (doi: 10.1109/IEDM50572.2025.11353799), IEEE International Electron Devices Meeting (IEDM) (Sep. 24, 2025)
- Top-Ranked Student Paper (doi: 10.1109/IEDM50572.2025.11353743), IEEE International Electron Devices Meeting (IEDM) (Sep. 24, 2025)
- Best Presentation Award, IEEE International Conference on Circuits, Systems, and Simulation (May 15, 2022)

- Best Paper Award, Institute of Electronics and Information Engineers (Dec. 31, 2020)

PROGRAM AFFILIATIONS

- Knight-Hennessy Scholars

EDUCATION AND CERTIFICATIONS

- M.S. degree, Seoul National University , electrical and computer engineering (2024)
- B.S. degree, Seoul National University , electrical and computer engineering (2018)

LINKS

- Personal Website: https://sites.google.com/view/yssong24
- Google Scholar: https://scholar.google.com/citations?user=vjaVM1QAAAAJ&hl=en

Professional

WORK EXPERIENCE

- Research Scientist - Semiconductor - IBM T. J. Watson Research Center (June 15, 2026 - September 4, 2026)
- Assistant Professor - Korea Military Academy - Department of Computer Science (September 9, 2021 - May 31, 2023)
- Full-Time Lecturer - Korea Military Academy - Department of Computer Science (June 1, 2020 - September 8, 2021)

Publications

PUBLICATIONS

- **Deep Learning to Automate Parameter Extraction and Model Fitting of Two-Dimensional Transistors** *RESEARCH*
  Bennett, R. K. A., Uslu, J., Gault, H. F., Khan, A., Hoang, L., Pena, T., Neilson, K., Song, Y., Zhang, Z., Mannix, A. J., Pop, E.
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- **Deep Learning to Automate Parameter Extraction and Model Fitting of Two-Dimensional Transistors.** *Research (Washington, D.C.)*
  Bennett, R. K., Uslu, J. L., Gault, H. F., Khan, A. I., Hoang, L., Peña, T., Neilson, K., Song, Y. S., Zhang, Z., Mannix, A. J., Pop, E.
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- **Scaling nanoribbon transistors with monolayer transition metal dichalcogenides.** *Nature nanotechnology*
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- **Structurally optimized SiC CMOS FinFET for high-temperature and low-power SoC logic integration** *SCIENTIFIC REPORTS*
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- **High-Field Breakdown and Thermal Characterization of Indium Tin Oxide Transistors.** *ACS nano*
  Su, H., Lee, Y., Pena, T., Fultz-Waters, S., Kang, J., Koroglu, C., Wahid, S., Newcomb, C. J., Song, Y. S., Wong, H. P., Wang, S. X., Pop, E.
  2025
- **Deep Learning to Automate Fitting and Parameter Extraction of 2D Transistors**
  Bennett, R. K. A., Gault, H. F., Khan, A., Hoang, L., Pena, T., Neilson, K., Song, Y., Zhang, Z., Mannix, A. J., Pop, E., IEEE
  IEEE.2025: 122-123
- **First Comparative Thermal Evaluation of 2D Semiconductor vs. Silicon Nanosheet Transistors**
  Song, Y., Su, H., Pena, T., Persson, A. E. O., Yang, K., Yalon, E., Bennett, R. K. A., Han, Z., Neilson, K., Kang, J., Yang, J. A., Wong, H., Wang, et al
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- **Thermal Evaluation and Comparison of CAA and GAA Indium Tin Oxide Vertical Channel Transistors**
  Song, Y., Kang, J., Gu, H., Su, H., Lee, Y., Wang, S. X., Kwon, J., Wong, H., Pop, E., IEEE

IEEE.2025

- **Analysis of thermal effects according to channel and drain contact metal distance** *CASE STUDIES IN THERMAL ENGINEERING*
  An, D., Lim, U., Song, Y., Kim, H., Kim, J.
  2025; 65

- **Optimization of FinFET's Fin Width and Height with Self-heating Effect** *JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE*
  Lee, G., Kwon, Y., Song, Y., Kim, H., Kim, J.
  2024; 24 (4): 365-372

- **Improvement of Thermal Characteristics and On-Current in Vertically Stacked Nanosheet FET by Parasitic Channel Height Engineering** *IEEE ACCESS*
  Song, Y., Kim, H., Hyun Kim, J.
  2024; 12: 105878-105886

- **Heterostructure performance evaluation: A numerical simulation and analytical modeling of the ferroelectric pocket doped double gate tunnel FET** *INTERNATIONAL JOURNAL OF NUMERICAL MODELLING-ELECTRONIC NETWORKS DEVICES AND FIELDS*
  Jeyanthi, J. E., Samuel, T., Song, Y., Venkatesh, M.
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- **Machine Learning Algorithm for Efficient Design of Separated Buffer Super-Junction IGBT** *MICROMACHINES*
  Kim, K., Hwang, T., Song, Y., Kim, H., Kim, J.
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- **Self-Heating and Interface Traps Assisted Early Aging Revelation and Reliability Analysis of Negative Capacitance FinFET**
  Jaisawal, R., Rathore, S., Gandhi, N., Kondekar, P. N., Banchhor, S., Sreenivas, V., Song, Y., Bagga, N., IEEE
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- **Self-Heating Aware Threshold Voltage Modulation Conforming to Process and Ambient Temperature Variation for Reliable Nanosheet FET**
  Rathore, S., Jaisawal, R., Kondekar, P. N., Gandhi, N., Banchhor, S., Song, Y., Bagga, N., IEEE
  IEEE.2023

- **Enhancement of Thermal Characteristics and On-Current in GAA MOSFET by Utilizing Al₂O₃-Based Dual-? Spacer Structure** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Song, Y., Kim, S., Kim, J., Kim, G., Lee, J., Choi, W.
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- **Incorporating Bottom-Up Approach Into Device/Circuit Co-Design for SRAM-Based Cache Memory Applications** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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- **Reliable High-Voltage Drain-Extended FinFET With Thermoelectric Improvement** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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- **Reliability improvement of self-heating effect, hot-carrier injection, and on-current variation by electrical/thermal co-design** *SOLID-STATE ELECTRONICS*
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  Kang, S., Kim, J., Song, Y., Go, S., Kim, S.
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- **Thermal-Aware IC Chip Design by Combining High Thermal Conductivity Materials and GAA MOSFET**

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- **Improvement of self-heating effect in Ge vertically stacked GAA nanowire pMOSFET by utilizing Al₂O₃ for high-performance logic device and electrical/thermal co-design** *JAPANESE JOURNAL OF APPLIED PHYSICS*
  Song, Y., Kim, S., Kim, G., Kim, H., Lee, J., Kim, J., Park, B.
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- **Improvement in Self-Heating Characteristic by Utilizing Sapphire Substrate in Omega-Gate-Shaped Nanowire Field Effect Transistor for Wearable, Military, and Aerospace Application.** *Journal of nanoscience and nanotechnology*
  Suh Song, Y., Kim, H., Yu, J., Lee, J.
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- **Erase Speed Enhancement with Low Power Operation by Incorporating Boron Doping** *JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE*
  Song, Y., Jang, T., Kim, H., Lee, J., Park, B.
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- **Retention Enhancement in Low Power NOR Flash Array with High-κ-Based Charge-Trapping Memory by Utilizing High Permittivity and High Bandgap of Aluminum Oxide** *MICROMACHINES*
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  Song, Y., Kim, J., Kim, G., Kim, H., Kim, S., Park, B.
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- **Tunneling oxide engineering for improving retention in nonvolatile charge-trapping memory with TaN/Al₂O₃/HfO₂/SiO₂/Al₂O₃/SiO₂/Si structure** *JAPANESE JOURNAL OF APPLIED PHYSICS*
  Song, Y., Jang, T., Min, K., Baek, M., Yu, J., Kim, Y., Lee, J., Park, B.
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- **Overflow Handling Integrate-and-Fire Silicon-on-Insulator Neuron Circuit Incorporating a Schmitt Trigger Implemented by Back-Gate Effect** *JOURNAL OF NANOSCIENCE AND NANOTECHNOLOGY*
  Kim, T., Song, Y., Park, B.
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