

Stanford



S Simon Wong

Professor of Electrical Engineering, Emeritus

CONTACT INFORMATION

- **Administrative Contact**

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Bio

BIO

Wong studies the fabrication and design of high-performance integrated circuits.

ACADEMIC APPOINTMENTS

- Emeritus Faculty, Acad Council, Electrical Engineering
- Member, Bio-X
- Member, Wu Tsai Neurosciences Institute

HONORS AND AWARDS

- Fellow, IEEE

BOARDS, ADVISORY COMMITTEES, PROFESSIONAL ORGANIZATIONS

- Adviser, Atheros Qualcomm (1998 - 2018)
- Board Director, Pericom Semiconductor (2006 - 2015)

PROGRAM AFFILIATIONS

- Stanford SystemX Alliance

PROFESSIONAL EDUCATION

- PhD, UC Berkeley (1983)

Teaching

STANFORD ADVISEES

Doctoral Dissertation Reader (AC)

George Alexopoulos

Publications

PUBLICATIONS

- **An international study presenting a federated learning AI platform for pediatric brain tumors.** *Nature communications*
Lee, E. H., Han, M., Wright, J., Kuwabara, M., Mevorach, J., Fu, G., Choudhury, O., Ratan, U., Zhang, M., Wagner, M. W., Goetti, R., Toescu, S., Perreault, et al
2024; 15 (1): 7615
- **Dimensional Scaling of Ferroelectric Properties of Hafnia-Zirconia Thin Films: Electrode Interface Effects.** *ACS nano*
Huang, F., Saini, B., Wan, L., Lu, H., He, X., Qin, S., Tsai, W., Gruverman, A., Meng, A. C., Wong, H. P., McIntyre, P. C., Wong, S.
2024
- **A New 1C1T1R nv-TCAM with Simultaneously Hybrid Ferroelectricity and Memristor Layers Feasible for Ultra-highly-dense and High-performance In-memory-searching**
Hsueh, Y. L., Lin, R. Q., Huang, Y. X., Lin, Y. H., Chang, K. H., Shen, T. H., Hsieh, E. R., Wong, S., IEEE
IEEE.2024: 103-105
- **Enhanced Switching Reliability of Hf_{0.5}Zr_{0.5}O₂ Ferroelectric Films Induced by Interface Engineering.** *ACS applied materials & interfaces*
Huang, F., Saini, B., Yu, Z., Yoo, C., Thampy, V., He, X., Baniecki, J. D., Tsai, W., Meng, A. C., McIntyre, P. C., Wong, S.
2023
- **First Observation of Ultra-high Polarization (~ 108 $\mu\text{C}/\text{cm}^2$) in Nanometer Scaled High Performance Ferroelectric HZO Capacitors with Mo Electrodes** *IEEE Symposium on VLSI Technology and Circuits*
Huang, F., Saini, B., Wan, L., Lu, H., He, X., Qin, S., Tsai, W., Gruverman, A., Meng, A., Wong, H., McIntyre, P., Wong, S.
2023
- **Foundry Monolithic 3D BEOL Transistor + Memory Stack: Iso-performance and Iso-footprint BEOL Carbon Nanotube FET+RRAM vs. FEOL Silicon FET+RRAM** *IEEE Symposium on VLSI Technology and Circuits*
Srimani, T., Yu, C., Radway, R., Rich, D., Nelson, M., Wong, S., Murphy, D., Fuller, S., Hills, g., Mitra, S., Shulaker, M.
2023
- **Measurement of Ferroelectric Properties of Nanometer Scaled Individual Metal/Hf_{0.5}Zr_{0.5}O₂/Metal Capacitors** *IEEE ELECTRON DEVICE LETTERS*
Huang, F., Passlack, M., Liew, S., Yu, Z., Lin, Q., Babadi, A., Hou, V., McIntyre, P. C., Wong, S.
2022; 43 (2): 212-215
- **4 Bits/cell Hybrid 1F1R for High Density Embedded Non-Volatile Memory and its Application for Compute in Memory** *IEEE Symposium on VLSI Technology and Circuits*
Chen, W., Huang, F., Qin, S., Yu, Z., Lin, Q., McIntyre, P., Wong, S., Wong, H.
2022
- **8-Layer 3D Vertical Ru/AIOxNy/TiN RRAM with Mega- Ω Level LRS for Low Power and Ultrahigh-density Memory** *IEEE Symposium on VLSI Technology and Circuits*
Qin, S., Tung, M., Belliveau, E., Liu, S., Kwon, J., Chen, W., Jiang, Z., Wong, S., Wong, H.
2022
- **RADAR: A Fast and Energy-Efficient Programming Technique for Multiple Bits-Per-Cell RRAM Arrays** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Le, B. Q., Levy, A., Wu, T. F., Radway, R. M., Hsieh, E., Zheng, X., Nelson, M., Raina, P., Wong, H., Wong, S., Mitra, S.
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- **3-D Vertical via Nitrogen-Doped Aluminum Oxide Resistive Random-Access Memory** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Lien, Y., Wu, T., Wong, S.
2021; 68 (6): 2712-2716
- **A FORMing-Free HfO₂/HfON-Based Resistive-Gate Metal-Oxide-Semiconductor Field-Effect-Transistor (RG-MOSFET) Nonvolatile Memory With 3-Bit-Per-Cell Storage Capability** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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- **Bidirectional Analog Conductance Modulation for RRAM-Based Neural Networks** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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- **A shallow convolutional neural network predicts prognosis of lung cancer patients in multi-institutional computed tomography image datasets** *Nature Machine Intelligence*
Mukherjee, P., Zhou, M., Lee, E., Schicht, A., Balagurunathan, Y., Napel, S., Gillies, R., Wong, S., Thieme, A., Leung, A., Gevaert, O.
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- **Next-Generation Ultrahigh-Density 3-D Vertical Resistive Switching Memory (VRSM)-Part I: Accurate and Computationally Efficient Modeling** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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- **Next-Generation Ultrahigh-Density 3-D Vertical Resistive Switching Memory (VRSM)-Part II: Design Guidelines for Device, Array, and Architecture** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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- **DATASET CULLING: TOWARDS EFFICIENT TRAINING OF DISTILLATION-BASED DOMAIN SPECIFIC MODELS**
Yoshioka, K., Lee, E., Wong, S., Horowitz, M., IEEE
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- **A Novel Architecture to Build Ideal-linearity Neuromorphic Synapses on a Pure Logic FinFET Platform Featuring 2.5ns PGM-time and 10(12) Endurance**
Hsieh, E. R., Chang, H. Y., Chung, S. S., Chen, T. P., Huang, S. A., Chen, T. J., Cheng, O., Wong, S., IEEE
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- **High-Density Multiple Bits-per-Cell 1T4R RRAM Array with Gradual SET/RESET and its Effectiveness for Deep Learning**
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- **Deep learning to predict survival prognosis for patients with non-small cell lung cancer using images and clinical data**
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- **Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM**
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- **Fault-Tolerant FPGA with Column-Based Redundancy and Power Gating Using RRAM** *IEEE TRANSACTIONS ON COMPUTERS*
Lee, K., Wong, S. S.
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- **Analysis and Design of a Passive Switched-Capacitor Matrix Multiplier for Approximate Computing** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
Lee, E. H., Wong, S. S.
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- **LOGNET: ENERGY-EFFICIENT NEURAL NETWORKS USING LOGARITHMIC COMPUTATION**
Lee, E. H., Miyashita, D., Chai, E., Murmann, B., Wong, S., IEEE

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- **A Deep Learning Framework to Predict Survival from Medical Images of Lung Cancer Patients** *Conference on Neural Information Processing Systems, Workshop on Machine Learning for Health*
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- **Switch Application in FPGA** *RESISTIVE SWITCHING: FROM FUNDAMENTALS OF NANOIONIC REDOX PROCESSES TO MEMRISTIVE DEVICE APPLICATIONS*
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- **All-Metal-Nitride RRAM Devices** *IEEE ELECTRON DEVICE LETTERS*
Zhang, Z., Gao, B., Fang, Z., Wang, X., Tang, Y., Sohn, J., Wong, H. P., Wong, S. S., Lo, G.
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- **FACTORIZATION FOR ANALOG-TO-DIGITAL MATRIX MULTIPLICATION**
Lee, E. H., Udell, M., Wong, S., IEEE
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- **The Role of Ti Capping Layer in HfO_x-Based RRAM Devices** *IEEE ELECTRON DEVICE LETTERS*
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2014; 35 (9): 912-914
- **Current Conduction Mechanism of Nitrogen-Doped AlO_x RRAM** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
Kim, W., Park, S. I., Zhang, Z., Wong, S.
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- **Low-Temperature Monolithic Three-Layer 3-D Process for FPGA** *IEEE ELECTRON DEVICE LETTERS*
Zhang, Z., Chen, C., Crnogorac, F., Chen, S., Griffin, P. B., Pease, R. F., Plummer, J. D., Wong, S. S.
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Park, J., Oh, S., Kim, S., Wong, H. P., Wong, S. S.
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Provine, J., Wong, H., Wong, S., Mitra, S.
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- **Scaling Challenges for the Cross-point Resistive Memory Array to the Single-digit-nm Node – An Interconnect Perspective**
Liang, S., Yip, S., Wong, H., S., Wong, P.
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- **Array Architecture for a Nonvolatile 3-Dimensional Cross-Point Resistance-Change Memory** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
Ou, E., Wong, S. S.
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- **A 60GHz Digitally Controlled RF Beamforming Array in 65nm CMOS with Off-Chip Antennas**
Lin, S., Ng, K., Wong, H., Luk, K., Wong, S., Poon, A.
2011
- **Forming-Free Nitrogen-Doped AlO_x RRAM with Sub- μ A Programming Current**
Kim, W., Park, S., I., Zhang, Z., Yang-Liau, Y., Sekar, D., Wong, H., S. P.
2011
- **3D Field Programmable Gate Array**
Yang-Liau, Y., Crnogorac, F., Chen, E., Jung, W., Kim, W., Park, S., Wong, S. S.
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- **Semiconductor crystal islands for three-dimensional integration** *54th International Conference on Electron, Ion and Photon Beam Technology and Nanofabrication*
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Jung, W. S., Park, J., Kuzum, D., Kim, W., Wong, S., Saraswat, K. C.
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- **A Low-Power V-Band CMOS Low Noise Amplifier using Current Sharing Technique**
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- **Monolithic 3D Integrated Circuits**
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2006
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