Stanford

Yuchen Mei

Ph.D. Student in Electrical Engineering, admitted Autumn 2023

Bio

BIO

Yuchen Mei is an EE Ph.D. student at Stanford University in Prof. Priyanka Raina's group. He received a B.S. degree in Electronic Information Science and Technology from Nanjing University (China) in 2021 and a M.S. degree in Electrical Engineering from Stanford in 2023. He is interested in digital VLSI design, domain-specific accelerators, and design automation.

EDUCATION AND CERTIFICATIONS

- Master of Science, Stanford University , Electrical Engineering (2023)
- Bachelor of Science, Nanjing University, China , Electronic Information Science and Technology (2021)

Publications

PUBLICATIONS

- **Opal: A 16-nm Coarse-Grained Reconfigurable Array SoC for Full Sparse Machine Learning Applications (vol 8, pg 293, 2025)** *IEEE SOLID-STATE CIRCUITS LETTERS*
  Chen, P., Cheng, B., Oduoza, M., Xie, Z., Lu, R., Ravipati, S., Koul, K., Carsello, A., Mei, Y., Horowitz, M., Raina, P.
  2026; 9: 141

- **Onyx: A 12-nm Programmable Accelerator for Dense and Sparse Applications** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Koul, K., Hsu, O., Mei, Y., Ravipati, S., Strange, M., Melchert, J., Carsello, A., Kong, T., Chen, P., Ke, H., Zhang, K., Liu, Q., Nyengele, et al
  2025

- **Opal: A 16-nm Coarse-Grained Reconfigurable Array SoC for Full Sparse Machine Learning Applications** *IEEE SOLID-STATE CIRCUITS LETTERS*
  Chen, P., Wun Cheng, B., Oduoza, M., Xie, Z., Lu, R., Gautham Ravipati, S., Koul, K., Carsello, A., Mei, Y., Horowitz, M., Raina, P.
  2025; 8: 293-296

- **Cascade: An Application Pipelining Toolkit for Coarse-Grained Reconfigurable Arrays** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Melchert, J., Mei, Y., Koul, K., Liu, Q., Horowitz, M., Raina, P.
  2024; 43 (10): 3055-3067

- **AHA: An Agile Approach to the Design of Coarse-Grained Reconfigurable Accelerators and Compilers** *ACM Transactions on Embedded Computing Systems*
  Koul, K., Melchert, J., Sreedhar, K., Truong, L., Nyengele, G., Zhang, K., Liu, Q., Setter, J., Chen, P., Mei, Y., Strange, M., Daly, R., Donovick, et al
  2023; 22 (2)

- **Canal: A Flexible Interconnect Generator for Coarse-Grained Reconfigurable Arrays** *IEEE Computer Architecture Letters*
  Melchert, J., Zhang, K., Mei, Y., Horowitz, M., Torng, C., Raina, P.
  2023

- **Temporal Residual Feature Learning for Efficient 3D Convolutional Neural Network on Action Recognition Task**
  Wang, H., Mei, Y., Lin, J., Wang, Z., IEEE
  IEEE.2020: 123-128

- **A Reconfigurable Permutation Based Address Encryption Architecture for Memory Security**
  Mei, Y., Du, L., He, X., Du, Y., Chen, X., Wang, Z., Reza, M., Sridhar, R.
  edited by Qu, G., Xiong, J., Zhao, D., Muthukumar
  IEEE.2020: 7-12