Stanford

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Bio

BIO

Po-Han Chen is an EE Ph.D. student at Stanford University supervised by Prof. Priyanka Raina. He received his B.S. in Electrical Engineering and Computer Science (EECS) and M.S. in Electrical Engineering from National Tsing Hua University (Taiwan) in 2016 and 2018 respectively. Before joining Stanford, he was a digital circuit designer at MediaTek where he worked on developing hardware architectures of image processing pipeline. He is interested in designing hardware accelerators. Most of his previous works were related to computational photography algorithms such as digital refocusing. Currently, He is focusing on analyzing and designing architecture of CGRAs to create high-performance, energy-efficient, and reconfigurable computing platforms.

Publications

PUBLICATIONS

- **Onyx: A 12-nm Programmable Accelerator for Dense and Sparse Applications** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
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- **Opal: A 16-nm Coarse-Grained Reconfigurable Array SoC for Full Sparse Machine Learning Applications** *IEEE SOLID-STATE CIRCUITS LETTERS*
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- **Amber: A 16-nm System-on-Chip With a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
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  Chen, P., Tsao, C., Raina, P., IEEE
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- **mflowgen: a modular flow generator and ecosystem for community-driven physical design** *DAC '22: Proceedings of the 59th ACM/IEEE Design Automation Conference*
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- **SAPIENS: A 64-kb RRAM-Based Non-Volatile Associative Memory for One-Shot Learning and Inference at the Edge** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
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