Stanford

Mark Horowitz

Fortinet Founders Chair of the Department of Electrical Engineering, Yahoo! Founders Professor in the School of Engineering and Professor of Computer Science

CONTACT INFORMATION

- **Administrative**

  Julie A. Hitchcock - Faculty Administrator

  Email julieh1@stanford.edu

  Tel 650.736.4454

Bio

BIO

Professor Horowitz initially focused on designing high-performance digital systems by combining work in computer-aided design tools, circuit design, and system architecture. During this time, he built a number of early RISC microprocessors, and contributed to the design of early distributed shared memory multiprocessors. In 1990, Dr. Horowitz took leave from Stanford to help start Rambus Inc., a company designing high-bandwidth memory interface technology. After returning in 1991, his research group pioneered many innovations in high-speed link design, and many of today's high speed link designs are designed by his former students or colleagues from Rambus.

In the 2000s he started a long collaboration with Prof. Levoy on computational photography, which included work that led to the Lytro camera, whose photographs could be refocused after they were captured.. Dr. Horowitz's current research interests are quite broad and span using EE and CS analysis methods to problems in neuro and molecular biology to creating new agile design methodologies for analog and digital VLSI circuits. He remains interested in learning new things, and building interdisciplinary teams.

ACADEMIC APPOINTMENTS

- Professor, Electrical Engineering
- Professor, Computer Science
- Member, Bio-X
- Affiliate, Precourt Institute for Energy
- Member, Wu Tsai Neurosciences Institute

ADMINISTRATIVE APPOINTMENTS

- Chair, Electrical Engineering Department, (2023- present)
- Vice Chair, 54th Senate of the Academic Council, (2021-2022)
- Steering Committee, 53rd Senate of the Academic Council, (2020-2021)
- Chair, Committee on Academic Computing and Information Systems (C-ACIS), (2019-2022)

- Chair, Electrical Engineering Department, (2008-2012)

HONORS AND AWARDS

- Elected Fellow, IEEE
- Elected Fellow, Association for Computing Machinery
- Eckert-Mauchly Award, ACM and IEEE Computer Society (2022)
- Faculty Researcher Award, SIA (2011)
- Donald O. Pederson Technical Field Award, IEEE (2006)
- Best Paper Award, ISQED (2005)
- Most Influential Paper of 1989, ISCA (2004)
- Jack Kilby Outstanding Paper Award, ISSCC (2003)
- Most influential paper, International Symposium of Computer Arch (1994)
- Best Paper Award, ISSCC (1993)
- Most Influential Paper, International Symposium on Computer Architecture (1989)
- Presidential Young Investigator Award, NSF (1985)

BOARDS, ADVISORY COMMITTEES, PROFESSIONAL ORGANIZATIONS

- Member, National Academy of Engineering (2013 - present)
- Member, Computer Science and Telecommunications Advisory Board, NAS (2013 - 2019)
- Member, American Academy of Arts and Sciences (2013 - present)

PROGRAM AFFILIATIONS

- Stanford SystemX Alliance

PROFESSIONAL EDUCATION

- PhD, Stanford University (1984)
- MS, MIT (1978)
- BS, MIT (1978)

PATENTS

- Gary B. Bronner, Brent S. Haukness, Mark A. Horowitz, Mark D. Kellam, Fariborz Assaderaghi. "United States Patent 11,244,727 Dynamic memory rank configuration", Rambus Inc, Feb 8, 2022
- Vladimir M Stojanovic, Andrew C Ho, Anthony Bessios, Bruno W Garlepp, Grace Tsang, Mark A Horowitz, Jared L Zerbe, Jason C Wei. "United States Patent 16/999,853 Partial response receiver", Rambus Inc, Mar 11, 2021
- Craig Hampel, Mark Horowitz. "United States Patent 17/000,130 System including hierarchical memory modules having different types of integrated circuit memory devices", Rambus Inc, Feb 4, 2021
- Mark Alan Horowitz, Ilias Pappas, Edward Buckley, William Thomas Blank. "United States Patent 10,861,380 Display systems with hybrid emitter circuits", Facebook Technologies LLC, Dec 8, 2020
- Haw-Jyh Liaw, Xingchao Yuan, Mark A Horowitz. "United States Patent 10,782,344 Technique for determining performance characteristics of electronic devices and systems", Rambus Inc, Sep 22, 2020
- Vladimir M Stojanovic, Andrew C Ho, Anthony Bessios, Fred F Chen, Elad Alon, Mark A Horowitz. "United States Patent 10,771,295 High speed signaling system with adaptive transmit pre-emphasis", Rambus Inc, Sep 8, 2020
- Vladimir M Stojanovic, Andrew C Ho, Anthony Bessios, Bruno W Garlepp, Grace Tsang, Mark A Horowitz, Jared L Zerbe, Jason C Wei. "United States Patent 10,764,094 Partial response receiver", Rambus Inc, Sep 1, 2020
- Craig Hampel, Mark Horowitz. "United States Patent 10,755,794 System including hierarchical memory modules having different types of integrated circuit memory devices", Rambus Inc, Aug 25, 2020

- Ely K Tsern, Mark A Horowitz, Frederick A Ware. "United States Patent 16/805,619 Memory Controller With Error Detection And Retry Modes Of Operation", Rambus Inc, Aug 20, 2020
- Ely K Tsern, Mark A Horowitz, Frederick A Ware. "United States Patent 10,621,023 Memory controller with error detection and retry modes of operation", Rambus Inc, Apr 14, 2020
- Vladimir M Stojanovic, Andrew C Ho, Anthony Bessios, Fred F Chen, Elad Alon, Mark A Horowitz. "United States Patent 10,411,923 High speed signaling system with adaptive transmit pre-emphasis", Rambus Inc, Sep 10, 2019
- Mark A Horowitz, Craig E Hampel, Alfredo Moncayo, Kevin S Donnelly, Jared L Zerbe. "United States Patent 10,366,045 Flash controller to provide a value that represents a parameter to a flash memory Inventors", Rambus Inc, Jul 30, 2019
- Noy Cohen, Marc S Levoy, Michael J Broxton, Logan Grosenick, Samuel Yang, Aaron Andalman, Karl A Disseroth, Mark A Horowitz. "United States Patent 10,317,597 Light-field microscopy with phase masking", Leland Stanford Junior University, Jun 11, 2019
- Jared LeVan Zerbe, Kevin S Donnelly, Stefanos Sidiropoulos, Donald C Stark, Mark A Horowitz, Leung Yu, Roxanne Vu, Jun Kim, Bruno W Garlepp, Tsyr-Chyang Ho, Benedict Chung-Kwong Lau. "United States Patent 10,310,999 Flash memory controller with calibrated data communication", Rambus Inc, Jun 4, 2019
- Jared L Zerbe, Bruno W Garlepp, Pak S Chau, Kevin S Donnelly, Mark A Horowitz, Stefanos Sidiropoulos, Billy W Garrett Jr, Carl W Werner. "United States Patent 9,998,305 Multi-PAM output driver with distortion compensation", Rambus Inc, Jun 12, 2018
- Haw-Jyh Liaw, Xingchao Yuan, Mark A Horowitz. "United States Patent 9,977,076 Technique for determining performance characteristics of electronic devices and systems", Rambus Inc, May 22, 2018
- Vladimir M Stojanovic, Andrew C Ho, Anthony Bessios, Bruno W Garlepp, Grace Tsang, Mark A Horowitz, Jared L Zerbe, Jason C Wei. "United States Patent 9,917,708 Partial response receiver", Rambus Inc, Mar 6, 2018

LINKS

- AHA! Agile Hardware Program: https://aha.stanford.edu/
- Stanford VLSI Research Group: https://vlsi.stanford.edu/

Teaching

COURSES

2025-26

- An Intro to Making: What is EE: ENGR 40M (Aut, Spr)
- Circuits I: EE 101A (Win)
- Design Projects in VLSI Systems I: EE 272 (Win)
- Digital Systems Engineering: EE 273 (Spr)

2024-25

- An Intro to Making: What is EE: ENGR 40M (Aut)
- Digital Systems Engineering: EE 273 (Spr)

2023-24

- An Intro to Making: What is EE: ENGR 40M (Aut, Win)

STANFORD ADVISEES

Doctoral Dissertation Reader (AC)

Po-Han Chen, Maximus Di Perna, Cristobal Eyzaguirre, Yao Hsiao, Wonsuk Jang, Aya Mouallem, Nikhil Poole, Ritvik Sharma, Haoran Xu, Megan Zeng

Orals Evaluator

Cristobal Eyzaguirre, Haoran Xu

Doctoral Dissertation Advisor (AC)

Taeyoung Kong, Gedeon Nyengele, Luke Sammarone, Maxwell Strange, Victor Turbiner, Can WANG

Doctoral (Program)

Brandon D'Agostino, Can WANG

Publications

PUBLICATIONS

- **Deconstruction of a spino-brain-spinal cord circuit drives chronic mechanical pain.** *Research square*
  Wang, Q., Lee, J. H., Nachtrab, G., Yuan, Y., Yuan, L., Qi, W., Mohr, M. A., Xiong, J., Horowitz, M. A., Chen, X.
  2025
- **Onyx: A 12-nm Programmable Accelerator for Dense and Sparse Applications** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Koul, K., Hsu, O., Mei, Y., Ravipati, S., Strange, M., Melchert, J., Carsello, A., Kong, T., Chen, P., Ke, H., Zhang, K., Liu, Q., Nyengele, et al
  2025
- **Designing Programmable Accelerators for Sparse Tensor Algebra** *IEEE MICRO*
  Koul, K., Xie, Z., Strange, M., Ravipati, S., Cheng, B., Hsu, O., Chen, P., Horowitz, M., Kjolstad, F., Raina, P.
  2025; 45 (3): 58-65
- **Opal: A 16-nm Coarse-Grained Reconfigurable Array SoC for Full Sparse Machine Learning Applications** *IEEE SOLID-STATE CIRCUITS LETTERS*
  Chen, P., Wun Cheng, B., Oduoza, M., Xie, Z., Lu, R., Gautham Ravipati, S., Koul, K., Carsello, A., Mei, Y., Horowitz, M., Raina, P.
  2025; 8: 293-296
- **A Probabilistic Perspective on Tiling Sparse Tensor Algebra**
  Sharma, R., Xue, Z., Zhang, N., Lacouture, R., Kjolstad, F., Achour, S., Horowitz, M., ACM
  ASSOC COMPUTING MACHINERY.2025: 795-808
- **Application of Formal Methods (SAT/SMT) to the Design of Constrained Codes**
  Sudhakaran, S., Barrett, C., Horowitz, M., IEEE
  IEEE.2025
- **Cascade: An Application Pipelining Toolkit for Coarse-Grained Reconfigurable Arrays** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Melchert, J., Mei, Y., Koul, K., Liu, Q., Horowitz, M., Raina, P.
  2024; 43 (10): 3055-3067
- **A 3.25 GHz Large-Integer Extended GCD Accelerator in 12 nm**
  Sreedhar, K., Nyengele, G., Horowitz, M., Torng, C., IEEE
  IEEE.2024: 476-479
- **Vision Transformer Computation and Resilience for Dynamic Inference**
  Sreedhar, K., Clemons, J., Venkatesan, R., Keckler, S. W., Horowitz, M., IEEE COMPUTER SOC
  IEEE COMPUTER SOC.2024: 192-204
- **Amber: A 16-nm System-on-Chip With a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Feng, K., Kong, T., Koul, K., Melchert, J., Carsello, A., Liu, Q., Nyengele, G., Strange, M., Zhang, K., Nayak, A., Setter, J., Thomas, J., Sreedhar, et al
  2023
- **Unified Buffer: Compiling Image Processing and Machine Learning Applications to Push-Memory Accelerators** *ACM Transactions on Architecture and Code Optimization*
  Liu, Q., Setter, J., Huff, D., Strange, M., Feng, K., Horowitz, M., Raina, P., Kjolstad, F.
  2023: 26
- **APEX: A Framework for Automated Processing Element Design Space Exploration using Frequent Subgraph Analysis** *ASPLOS 2023: Proceedings of the 28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems*
  Melchert, J., Feng, K., Donovick, C., Daly, R., Sharma, R., Barrett, C., Horowitz, M., Hanrahan, P., Raina, P.
  2023
- **Hardware Abstractions and Hardware Mechanisms to Support Multi-Task Execution on Coarse-Grained Reconfigurable Arrays** *arXiv*
  Kong, T., Koul, K., Raina, P., Horowitz, M., Torng, C.

2023

- **Canal: A Flexible Interconnect Generator for Coarse-Grained Reconfigurable Arrays** *IEEE Computer Architecture Letters*
  Melchert, J., Zhang, K., Mei, Y., Horowitz, M., Torng, C., Raina, P.
  2023
- **AHA: An Agile Approach to the Design of Coarse-Grained Reconfigurable Accelerators and Compilers** *ACM Transactions on Embedded Computing Systems*
  Koul, K., Melchert, J., Sreedhar, K., Truong, L., Nyengele, G., Zhang, K., Liu, Q., Setter, J., Chen, P., Mei, Y., Strange, M., Daly, R., Donovick, et al
  2023; 22 (2)
- **Higher education's influence on social networks and entrepreneurship in Brazil** *SOCIAL NETWORK ANALYSIS AND MINING*
  Reddy, M., Nardelli, J. C., Pereira, Y. L., Oliveira, L. B., Silva, T. H., Vasconcelos, M., Horowitz, M.
  2022; 13 (1)
- **An Open-Source Framework for FPGA Emulation of Analog/Mixed-Signal Integrated Circuit Designs** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Herbst, S., Rutsch, G., Ecker, W., Horowitz, M.
  2022; 41 (7): 2223-2236
- **Improving Energy Efficiency of CGRAs with Low-Overhead Fine-Grained Power Domains** *ACM Transactions on Reconfigurable Technology and Systems*
  Nayak, A., Zhang, K., Setaluri, R., Carsello, A., Mann, M., Torng, C., Richardson, S., Bahr, R., Hanrahan, P., Horowitz, M., Raina, P.
  2022
- **Enabling and Accelerating Dynamic Vision Transformer Inference for Real-Time Applications** *arXiv*
  Sreedhar, K., Clemons, J., Venkatesan, R., Keckler, S. W., Horowitz, M.
  2022
- **Cascade: An Application Pipelining Toolkit for Coarse-Grained Reconfigurable Arrays** *arXiv*
  Melchert, J., Mei, Y., Koul, K., Liu, Q., Horowitz, M., Raina, P.
  2022
- **The Sparse Abstract Machine** *arXiv*
  Hsu, O., Strange, M., Won, J., Sharma, R., Olukotun, K., Emer, J., Horowitz, M., Kjolstad, F.
  2022
- **Amber: Coarse-Grained Reconfigurable Array-Based SoC for Dense Linear Algebra Acceleration** *2022 IEEE Hot Chips 34 Symposium (HCS)*
  Feng, K., et al
  2022: 1-30
- **mflowgen: a modular flow generator and ecosystem for community-driven physical design** *DAC '22: Proceedings of the 59th ACM/IEEE Design Automation Conference*
  Carsello, A., Thomas, J., Nayak, A., Chen, P., Horowitz, M., Raina, P., Torng, C.
  2022: 1339–1342
- **Bringing source-level debugging frameworks to hardware generators** *DAC '22: Proceedings of the 59th ACM/IEEE Design Automation Conference*
  Zhang, K., Asgar, Z., Horowitz, M.
  2022: 1171–1176
- **Amber: A 367 GOPS, 538 GOPS/W 16nm SoC with a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra** *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*
  Carsello, A., et al
  2022
- **Automating System Configuration** *CONFERENCE ON FORMAL METHODS IN COMPUTER-AIDED DESIGN–FMCAD 2021*
  Tsiskaridze, N., Strange, M., Mann, M., Sreedhar, K., Liu, Q., Horowitz, M., Barrett, C.
  2021
- **Online, Interactive Tool for Studying How Students Troubleshoot Circuits** *2021 ASEE Virtual Annual Conference*

Fritz, A., Horowitz, M., Jha, A.
2021

- **Compiling Halide Programs to Push-Memory Accelerators** *arXiv.org (https://arxiv.org/abs/2105.12858)*
  Liu, Q., Huff, D., Setter, J., Strange, M., Feng, K., Sreedhar, K., Wang, Z., Zhang, K., Horowitz, M., Raina, P., Kjolstad, F.
  2021
- **Automated Design Space Exploration of CGRA Processing Element Architectures using Frequent Subgraph Analysis** *arXiv.org (https://arxiv.org/abs/2104.14155)*
  Melchert, J., Feng, K., Donovick, C., Daly, R., Barrett, C., Horowitz, M., Hanrahan, P., Raina, P.
  2021
- **A Fast Large-Integer Extended GCD Algorithm and Hardware Design for Verifiable Delay Functions and Modular Inversion** *Cryptology ePrint Archive*
  Sreedhar, K., Horowitz, M., Torng, C.
  2021
- **Enabling Reusable Physical Design Flows with Modular Flow Generators** *arXiv.org*
  Carsello, A., Thomas, J., Nayak, A., Chen, P., Horowitz, M., Raina, P., Torng, C.
  2021
- **Fast Validation of Mixed-Signal SoCs** *IEEE Open Journal of the Solid-State Circuits Society*
  Stanley, D., Wang, C., Kim, S., Herbst, S., Kim, J., Horowitz, M.
  2021; 1: 184 - 195
- **fault: A Python Embedded Domain-Specific Language for Metaprogramming Portable Hardware Verification Components** *International Conference on Computer Aided Verification*
  Truong, L., Herbst, S., Setaluri, R., Mann, M., Daly, R., Zhang, K., Donovick, C., Stanley, D., Horowitz, M., Barrett, C., Hanrahan, P.
  2020
- **Interstellar: Using Halide's Scheduling Language to Analyze DNN Accelerators**
  Yang, X., Gao, M., Liu, Q., Setter, J., Pu, J., Nayak, A., Bell, S., Cao, K., Ha, H., Raina, P., Kozyrakis, C., Horowitz, M., ACM
  ASSOC COMPUTING MACHINERY.2020: 369–83
- **20-GS/s 8-bit Analog-to-Digital Converter and 5-GHz Phase Interpolator for Open-Source Synthesizable High-Speed Link Applications** *IEEE Solid-State Circuits Letters*
  Kim, S., Myers, Z., Herbst, S., Lim, B., Horowitz, M.
  2020; 3: 518 - 521
- **SegAlign: A Scalable GPU-Based Whole Genome Aligner** *International Conference for High Performance Computing, Networking, Storage and Analysis (SC)*
  Goenka, S., Turakhia, Y., Paten, B., Horowitz, M.
  2020: 540–552
- **Creating an Agile Hardware Design Flow** *2020 57th ACM/IEEE Design Automation Conference (DAC)*
  Bahr, R., Barrett, C., Bhagdikar, N., Carsello, A., Daly, R., Donovick, C., Durst, D., Fatahalian, K., Feng, K., Hanrahan, P., Hofstee, T., Horowitz, M., Huff, et al
  2020
- **A Framework for Adding Low-Overhead, Fine-Grained Power Domains to CGRAs**
  Nayak, A., Zhang, K., Setaluri, R., Carsello, A., Mann, M., Richardson, S., Bahr, R., Hanrahan, P., Horowitz, M., Raina, P.
  Design, Automation and Test in Europe Conference (DATE).
  2020
- **Open-Source Synthesizable Analog Blocks for High-Speed Link Designs: 20-GS/s 5b ENOB Analog-to-Digital Converter and 5-GHz Phase Interpolator** *2020 IEEE Symposium on VLSI Circuits*
  Kim, S., Myers, Z., Herbst, S., Lim, B., Horowitz, M.
  2020
- **An Analog Model Template Library: Simplifying Chip-Level, Mixed-Signal Design Verification** *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS*

Lim, B., Horowitz, M.
2019; 27 (1): 193–204

- **Quantum Computing's Implications for Cryptography** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
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  2019: 95–112

- **Quantum Algorithms and Applications** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  edited by Grumbling, E., Horowitz, M.
  2019: 57–94

- **QUANTUM COMPUTING Progress and Prospects Summary** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  edited by Grumbling, E., Horowitz, M.
  2019: 1–11

- **Other Approaches to Building Qubits** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  edited by Grumbling, E., Horowitz, M.
  2019: 212–25

- **Statement of Task** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  edited by Grumbling, E., Horowitz, M.
  2019: 195

- **Essential Hardware Components of a Quantum Computer** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  edited by Grumbling, E., Horowitz, M.
  2019: 113–34

- **Essential Software Components of a Scalable Quantum Computer** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  edited by Grumbling, E., Horowitz, M.
  2019: 135–55

- **Global R&D Investment** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
  edited by Grumbling, E., Horowitz, M.
  2019: 226–29

- **Quantum Computing: A New Paradigm** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
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  2019: 24–56

- **Falcon — A Flexible Architecture For Accelerating Cryptography** *2019 IEEE 16th International Conference on Mobile Ad Hoc and Sensor Systems (MASS)*
  Kiningham, K., Levis, P., Anderson, M., Boneh, D., Horowitz, M., Shih, M.

2019

- **QUANTUM COMPUTING Progress and Prospects Summary** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
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- **Statement of Task** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
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  edited by Grumbling, E., Horowitz, M.
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- **Essential Hardware Components of a Quantum Computer** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
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- **Quantum Computing: A New Paradigm** *QUANTUM COMPUTING: PROGRESS AND PROSPECTS*
  Horowitz, M. A., Aspuru-Guzik, A., Awschalom, D. D., Blakley, B., Boneh, D., Coppersmith, S. N., Kim, J., Martinis, J. M., Martonosi, M., Mosca, M., Oliver, W. D., Svore, K., Vazirani, et al
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  2019: 24–56

- **Falcon — A Flexible Architecture For Accelerating Cryptography** *2019 IEEE 16th International Conference on Mobile Ad Hoc and Sensor Systems (MASS)*
  Kiningham, K., Levis, P., Anderson, M., Boneh, D., Horowitz, M., Shih, M.
  2019

- **Mapping Histological Slice Sequences to the Allen Mouse Brain Atlas Without 3D Reconstruction.** *Frontiers in neuroinformatics*
  Xiong, J., Ren, J., Luo, L., Horowitz, M.
  2018; 12: 93

- **Mapping Histological Slice Sequences to the Allen Mouse Brain Atlas Without 3D Reconstruction** *FRONTIERS IN NEUROINFORMATICS*
  Xiong, J., Ren, J., Luo, L., Horowitz, M.
  2018; 12

- **Anatomically Defined and Functionally Distinct Dorsal Raphe Serotonin Sub-systems** *CELL*
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PRESENTATIONS

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