Stanford



H.-S. Philip Wong

Willard R. and Inez Kerr Bell Professor in the School of Engineering

Electrical Engineering

CONTACT INFORMATION

- **Alternate Contact**

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Bio

BIO

H.-S. Philip Wong is the Willard R. and Inez Kerr Bell Professor in the School of Engineering at Stanford University. He joined Stanford University as Professor of Electrical Engineering in 2004. From 1988 to 2004, he was with the IBM T.J. Watson Research Center. From 2018 to 2020, he was on leave from Stanford and was the Vice President of Corporate Research at TSMC, the largest semiconductor foundry in the world, and since 2020 remains the Chief Scientist of TSMC in a consulting, advisory role.

He is a member of the National Academy of Engineering and a Fellow of the IEEE. He received the IEEE Andrew S. Grove Award, the IEEE Technical Field Award to honor individuals for outstanding contributions to solid-state devices and technology, as well as the IEEE Electron Devices Society J.J. Ebers Award, the society's highest honor to recognize outstanding technical contributions to the field of electron devices that have made a lasting impact.

He is the Principal Investigator of the Microelectronics Commons California-Pacific-Northwest AI Hardware Hub, a consortium of over 60 companies and academic institutions funded by the CHIPS Act. He was a member of the US Department of Commerce Industrial Advisory Committee on microelectronics. He serves on the Executive Committee of the UC Berkeley think tank Technology Competitiveness and Industrial Policy (TCIP) Center.

ACADEMIC APPOINTMENTS

- Professor, Electrical Engineering
- Member, Bio-X
- Affiliate, Precourt Institute for Energy
- Member, Wu Tsai Neurosciences Institute

ADMINISTRATIVE APPOINTMENTS

- Director, Stanford Nanofabrication Facility, (2021-2024)

HONORS AND AWARDS

- Member, National Academy of Engineering (2026)
- Fellow, IEEE (2001)

PROGRAM AFFILIATIONS

- Stanford SystemX Alliance

PROFESSIONAL EDUCATION

- PhD, Lehigh (1988)

LINKS

- http://nano.stanford.edu: http://nano.stanford.edu
- https://web.stanford.edu/~hspwong: https://web.stanford.edu/~hspwong

Teaching

COURSES

2026-27

- Advanced VLSI Devices: EE 316 (Win)
- Making at the Nanometer Scale: A Journey into Microchips: EE 21N (Win)

2025-26

- Emerging Non-Volatile Memory Devices and Circuit Design: EE 309B (Win)
- Making at the Nanometer Scale: A Journey into Microchips: EE 21N (Win)
- Semiconductor Memory Devices and Circuit Design: EE 309A (Aut)

2024-25

- Advanced VLSI Devices: EE 316 (Win)
- Making at the nanometer scale: A journey into microchips: EE 21N (Win)

2023-24

- Emerging Non-Volatile Memory Devices and Circuit Design: EE 309B (Win)
- Making at the nanometer scale: A journey into microchips: EE 21N (Win)
- Semiconductor Memory Devices and Circuit Design: EE 309A (Aut)

STANFORD ADVISEES

Doctoral Dissertation Reader (AC)

Suhyeong Choi, Yeongmin Park, Young Suh Song, Jennifer Toy

Postdoctoral Faculty Sponsor

Fabia Farlin Athena, Chi-Hsin Huang, Xinxin Wang

Doctoral Dissertation Advisor (AC)

Hugo Chen, Jack Evans, Koustav Jana, Jimin Kang, Shuhan Liu, Mary Petty, Jimmy Qin, Samantha van Rijs

Master's Program Advisor

Stephanie Chang, Jing Chen, Archer Date, Christian Kubicka, Anderson Truong, Anya Wang, Yang Wang, Mike Zhao, Jin Zhou

Doctoral (Program)

Jimin Kang, Shuhan Liu, Jimmy Qin, Yiming Tan, Andrew Yang

Publications

PUBLICATIONS

- **Rapid Co-Optimization of Processing and Circuit Design to Overcome Carbon Nanotube Variations** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Hills, G., Zhang, J., Shulaker, M. M., Wei, H., Lee, C., Balasingam, A., Wong, H. P., Mitra, S.
  2015; 34 (7): 1082-1095

- **1D Selection Device Using Carbon Nanotube FETs for High-Density Cross-Point Memory Arrays** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Ahn, C., Jiang, Z., Lee, C., Chen, H., Liang, J., Liyanage, L. S., Wong, H. P.
  2015; 62 (7): 2197-2204

- **Partitioning Electrostatic and Mechanical Domains in Nanoelectromechanical Relays** *JOURNAL OF MICROELECTROMECHANICAL SYSTEMS*
  Shavezipur, M., Harrison, K., Lee, W. S., Mitra, S., Wong, H. P., Howe, R. T.
  2015; 24 (3): 592-598

- **Large-Area Assembly of Densely Aligned Single-Walled Carbon Nanotubes Using Solution Shearing and Their Application to Field-Effect Transistors** *ADVANCED MATERIALS*
  Park, S., Pitner, G., Giri, G., Koo, J. H., Park, J., Kim, K., Wang, H., Sinclair, R., Wong, H. P., Bao, Z.
  2015; 27 (16): 2656-2662

- **A General Design Strategy for Block Copolymer Directed Self-Assembly Patterning of Integrated Circuits Contact Holes using an Alphabet Approach.** *Nano letters*
  Yi, H., Bao, X., Tiberio, R., Wong, H. P.
  2015; 15 (2): 805-812

- **Continuous wireless pressure monitoring and mapping with ultra-small passive sensors for health monitoring and critical care** *NATURE COMMUNICATIONS*
  Chen, L. Y., Tee, B. C., Chortos, A. L., Schwartz, G., Tse, V., Lipomi, D. J., Wong, H. P., McConnell, M. V., Bao, Z.
  2014; 5

- **Carbon nanotubes for high-performance logic** *MRS BULLETIN*
  Chen, Z., Wong, H. P., Mitra, S., Bol, A., Peng, L., Hills, G., Thissen, N.
  2014; 39 (8): 719-726

- **Improved Performance of Bottom-Contact Organic Thin-Film Transistor Using Al Doped HfO2 Gate Dielectric** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Tang, W. M., Aboudi, U., Provine, J., Howe, R. T., Wong, H. P.
  2014; 61 (7): 2398-2403

- **Ultrafast terahertz-induced response of GeSbTe phase-change materials** *APPLIED PHYSICS LETTERS*
  Shu, M. J., Zalden, P., Chen, F., Weems, B., Chatzakis, I., Xiong, F., Jeyasingh, R., Hoffmann, M. C., Pop, E., Wong, H. P., Wuttig, M., Lindenberg, A. M.
  2014; 104 (25)

- **Ultrafast characterization of phase-change material crystallization properties in the melt-quenched amorphous phase.** *Nano letters*
  Jeyasingh, R., Fong, S. W., Lee, J., Li, Z., Chang, K., Mantegazza, D., Asheghi, M., Goodson, K. E., Wong, H. P.
  2014; 14 (6): 3419-3426

- **Multi-level control of conductive nano-filament evolution in HfO2 ReRAM by pulse-train operations** *NANOSCALE*
  Zhao, L., Chen, H., Wu, S., Jiang, Z., Yu, S., Hou, T., Wong, H. P., Nishi, Y.
  2014; 6 (11): 5698-5702

- **Cost-Effective, Transfer-Free, Flexible Resistive Random Access Memory Using Laser-Scribed Reduced Graphene Oxide Patterning Technology** *NANO LETTERS*
  Tian, H., Chen, H., Ren, T., Li, C., Xue, Q., Mohammad, M. A., Wu, C., Yang, Y., Wong, H. P.
  2014; 14 (6): 3214-3219

- **Computer-Aided Diagnosis of Hyperacute Stroke with Thrombolysis Decision Support Using a Contralateral Comparative Method of CT Image Analysis** *JOURNAL OF DIGITAL IMAGING*
  Shieh, Y., Chang, C., Shieh, M., Lee, T., Chang, Y. J., Wong, H., Chin, S. C., Goodwin, S.
  2014; 27 (3): 392-406

- **3-D Cross-Point Array Operation on AlOy/HfOx-Based Vertical Resistive Switching Memory** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Gao, B., Chen, B., Liu, R., Zhang, F., Huang, P., Liu, L., Liu, X., Kang, J., Chen, H. (., Yu, S., Wong, H. P.
  2014; 61 (5): 1377-1381

- **System Level Benchmarking with Yield-Enhanced Standard Cell Library for Carbon Nanotube VLSI Circuits** *ACM JOURNAL ON EMERGING TECHNOLOGIES IN COMPUTING SYSTEMS*
  Bobba, S., Zhang, J., Gaillardon, P., Wong, H. P., Mitra, S., De Micheli, G.
  2014; 10 (4)

- **VLSI-Compatible Carbon Nanotube Doping Technique with Low Work-Function Metal Oxides.** *Nano letters*
  Suriyasena Liyanage, L., Xu, X., Pitner, G., Bao, Z., Wong, H. P.
  2014; 14 (4): 1884-1890

- **Carbon Nanotube Circuit Integration up to Sub-20 nm Channel Lengths** *ACS NANO*
  Shulaker, M. M., Van Rethy, J., Wu, T. F., Liyanage, L. S., Wei, H., Li, Z., Pop, E., Gielen, G., Wong, H. P., Mitra, S.
  2014; 8 (4): 3434-3443

- **GaAs buffer layer technique for vertical nanowire growth on Si substrate** *APPLIED PHYSICS LETTERS*
  Xu, X., Li, Y., Parizi, K. B., Huo, Y., Kang, Y., Wong, H. P.
  2014; 104 (8)

- **Sensor-to-Digital Interface Built Entirely With Carbon Nanotube FETs**
  Shulaker, M. M., Rethy, J. V., Hills, G., Wei, H., Chen, H. Y., Gielen, G., Wong, H.S.Philip
  2014

- **Statistical Assessment Methodology for the Design and Optimization of Cross-Point RRAM Arrays** *IEEE 6th International Memory Workshop (IMW)*
  Li, H., Jiang, Z., Huang, P., Chen, H., Chen, B., Liu, R., Chen, Z., Zhang, F., Liu, L., Gao, B., Liu, X., Yu, S., Wong, et al
  IEEE.2014

- **Electrochemical Metallization and Trapping/Detrapping Resistive Switching Mechanism in Al/VOx/Cu RRAM** *ECS SOLID STATE LETTERS*
  Zhang, K., Sun, K., Wang, F., Han, Y., Jiang, Z., Wang, B., Liu, K., Wong, H. S.
  2014; 3 (10): Q63-Q66

- **Directed Self-Assembly (DSA) Template Pattern Verification** *51st ACM/EDAC/IEEE Design Automation Conference (DAC)*
  Xiao, Z., Du, Y., Tian, H., Wong, M. D., Yi, H., Wong, H. P., Zhang, H.
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- **DSA Template Optimization for Contact Layer in 1D Standard Cell Design** *Conference on Alternative Lithographic Technologies VI*
  Xiao, Z., Du, Y., Tian, H., Wong, M. D., Yi, H., Wong, H. P.
  SPIE-INT SOC OPTICAL ENGINEERING.2014

- **Write Disturb Analyses on Half-Selected Cells of Cross-Point RRAM Arrays** *International Reliability Physics Symposium (IRPS)*
  Li, H., Chen, H., Chen, Z., Chen, B., Liu, R., Qiu, G., Huang, P., Zhang, F., Jiang, Z., Gao, B., Liu, L., Liu, X., Yu, et al
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- **Optimization and Mechanism on Chemical Mechanical Planarization of Hafnium Oxide for RRAM Devices** *ECS JOURNAL OF SOLID STATE SCIENCE AND TECHNOLOGY*
  Zhang, K., Feng, Y., Cao, J., Wang, F., Han, Y., Yuan, Y., Wong, H. S.

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- **DSA-Aware Detailed Routing for Via Layer Optimization** *Conference on Alternative Lithographic Technologies VI*
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- **Oral and topical boswellic acid attenuates mouse osteoarthritis** *OSTEOARTHRITIS AND CARTILAGE*
  Wang, Q., Pan, X., Wong, H. H., Wagner, C. A., Lahey, L. J., Robinson, W. H., Sokolove, J.
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- **Brain-like associative learning using a nanoscale non-volatile phase change synaptic device array.** *Frontiers in neuroscience*
  Eryilmaz, S. B., Kuzum, D., Jeyasingh, R., Kim, S., BrightSky, M., Lam, C., Wong, H. P.
  2014; 8: 205-?
- **Sensor-to-Digital Interface Built Entirely With Carbon Nanotube FETs** *IEEE JOURNAL OF SOLID-STATE CIRCUITS*
  Shulaker, M. M., Van Rethy, J., Hills, G., Wei, H., Chen, H., Gielen, G., Wong, H. P., Mitra, S.
  2014; 49 (1): 190-201
- **System Level Benchmarking with Yield-Enhanced Standard Cell Library for Carbon Nanotube VLSI Circuits** *ACM Journal on Emerging Technologies in Computing Systems*
  Mitra, S., Gaillardon, P. E., Micheli, G. D., Wong, H. S., Bobba, S., Zhang, J.
  2014
- **Experimental study of plane electrode thickness scaling for 3D vertical resistive random access memory.** *Nanotechnology*
  Chen, H., Yu, S., Gao, B., Liu, R., Jiang, Z., Deng, Y., Chen, B., Kang, J., Philip Wong, H.
  2013; 24 (46): 465201-?
- **Assembly and Installation of the Daya Bay Antineutrino Detectors** *JOURNAL OF INSTRUMENTATION*
  Band, H. R., Brown, R. L., Carr, R., Chen, X. C., Chen, X. H., CHERWINKA, J. J., Chu, M. C., Draeger, E., Dwyer, D. A., Edwards, W. R., Gill, R., Goett, J., Greenler, et al
  2013; 8
- **Synergetic carbon nanotube growth** *CARBON*
  Parker, J. M., Wong, H. P.
  2013; 62: 61-68
- **Synaptic electronics: materials, devices and applications** *NANOTECHNOLOGY*
  Kuzum, D., Yu, S., Wong, H. P.
  2013; 24 (38)
- **Nanometer-Scale HfOx RRAM** *IEEE ELECTRON DEVICE LETTERS*
  Zhang, Z., Wu, Y., Wong, H. P., Wong, S. S.
  2013; 34 (8): 1005-1007
- **Mass fabrication and delivery of 3D multilayer mu Tags into living cells** *SCIENTIFIC REPORTS*
  Chen, L. Y., Parizi, K. B., Kosuge, H., Milaninia, K. M., McConnell, M. V., Wong, H. P., Poon, A. S.
  2013; 3
- **Impact of III-V and Ge Devices on Circuit Performance** *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS*
  Park, J., Oh, S., Kim, S., Wong, H. P., Wong, S. S.
  2013; 21 (7): 1189-1200
- **Atomic layer deposition of high-k dielectrics on single-walled carbon nanotubes: a Raman study** *NANOTECHNOLOGY*
  Liyanage, L. S., Cott, D. J., Delabie, A., Van Elshocht, S., Bao, Z., Wong, H. P.
  2013; 24 (24)
- **Compact Model for Carbon Nanotube Field-Effect Transistors Including Nonidealities and Calibrated With Experimental Data Down to 9-nm Gate Length** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Luo, J., Wei, L., Lee, C., Franklin, A. D., Guan, X., Pop, E., Antoniadis, D. A., Wong, H. P.
  2013; 60 (6): 1834-1843

- **Phonon and electron transport through Ge2Sb2Te5 films and interfaces bounded by metals** *APPLIED PHYSICS LETTERS*
  Lee, J., Bozorg-Grayeli, E., Kim, S., Asheghi, M., Wong, H. P., Goodson, K. E.
  2013; 102 (19)
- **Combinational Logic Design Using Six-Terminal NEM Relays** *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*
  Lee, D., Lee, W. S., Chen, C., Fallah, F., Provine, J., Chong, S., Watkins, J., Howe, R. T., Wong, H. P., Mitra, S.
  2013; 32 (5): 653-666
- **A Low Energy Oxide-Based Electronic Synaptic Device for Neuromorphic Visual Systems with Tolerance to Device Variation** *ADVANCED MATERIALS*
  Yu, S., Gao, B., Fang, Z., Yu, H., Kang, J., Wong, H. P.
  2013; 25 (12): 1774-1779
- **HfOx-Based Vertical Resistive Switching Random Access Memory Suitable for Bit-Cost-Effective Three-Dimensional Cross-Point Architecture** *ACS NANO*
  Yu, S., Chen, H., Gao, B., Kang, J., Wong, H. P.
  2013; 7 (3): 2320-2325
- **Monitoring Oxygen Movement by Raman Spectroscopy of Resistive Random Access Memory with a Graphene-Inserted Electrode** *NANO LETTERS*
  Tian, H., Chen, H., Gao, B., Yu, S., Liang, J., Yang, Y., Xie, D., Kang, J., Ren, T., Zhang, Y., Wong, H. P.
  2013; 13 (2): 651-657
- **Effect of Wordline/Bitline Scaling on the Performance, Energy Consumption, and Reliability of Cross-Point Memory Array** *ACM JOURNAL ON EMERGING TECHNOLOGIES IN COMPUTING SYSTEMS*
  Liang, J., Yeh, S., Wong, S. S., Wong, H. P.
  2013; 9 (1)
- **Design Strategy of Small Topographical Guiding Templates for sub-15 nm Integrated Circuits Contact Hole Patterns using Block Copolymer Directed Self-Assembly** *Conference on Alternative Lithographic Technologies V*
  Yi, H., Bao, X., Tiberio, R., Wong, H. P.
  SPIE-INT SOC OPTICAL ENGINEERING.2013
- **< span> Phase Change Memory–The Interplay Between Thermal and Electrical Effects**
  Wong, H. S.
  2013
- **Carbon nanotube circuits: opportunities and challenges**
  Wei, H., Shulaker, M., Hills, G., Chen, H. Y., Lee, C. S., Liyanage, L., Wong, H.S.Philip
  2013
- **Phonon and electron transport through Ge 2 Sb 2 Te 5 films and interfaces bounded by metals** *Applied Physics Letters*
  Lee, J., Bozorg-Grayeli, E., Kim, S. B., Asheghi, M., Wong, H. P., Goodson, K. E.
  2013; 19 (102): 191911-191911-5
- **Rapid exploration of processing and design guidelines to overcome carbon nanotube variations**
  Hills, G., Zhang, J., Mackin, C., Shulaker, M., Wei, H., Wong, H. S.
  2013
- **Sacha: the Stanford Carbon Nanotube Controlled Handshaking Robot** *50th ACM/EDAC/IEEE Design Automation Conference (DAC)*
  Shulaker, M., Van Rethy, J., Hills, G., Chen, H., Gielen, G., Wong, H. P., Mitra, S.
  IEEE COMPUTER SOC.2013
- **Reliability of Graphene Interconnects and N-type Doping of Carbon Nanotube transistors** *IEEE International Reliability Physics Symposium (IRPS)*
  Liyanage, L. S., Chen, X., Wei, H., Chen, H., Mitra, S., Wong, H. P.
  IEEE.2013
- **Design and Optimization Methodology for 3D RRAM Arrays** *IEEE International Electron Devices Meeting (IEDM)*
  Deng, Y., Chen, H., Gao, B., Yu, S., Wu, S., Zhao, L., Chen, B., Jiang, Z., Liu, X., Hou, T., Nishi, Y., Kang, J., Wong, et al

IEEE.2013

- **Monolithic Three-Dimensional Integration of Carbon Nanotube FET Complementary Logic Circuits** *IEEE International Electron Devices Meeting (IEDM)*
  Wei, H., Shulaker, M., Wong, H. P., Mitra, S.
  IEEE.2013
- **First Demonstration of RRAM Patterned by Block Copolymer Self-Assembly** *IEEE International Electron Devices Meeting (IEDM)*
  Wu, Y., Yi, H., Zhang, Z., Jiang, Z., Sohn, J., Wong, S., Wong, H. P.
  IEEE.2013
- **LATERALLY ACTUATED NANOELECTROMECHANICAL RELAYS WITH COMPLIANT, LOW RESISTANCE CONTACT** *26th IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*
  Shavezipur, M., Lee, W. S., Harrison, K. L., Provine, J., Mitra, S., Wong, H. P., Howe, R. T.
  IEEE.2013: 520–523
- **Experimental Demonstration of Array-level Learning with Phase Change Synaptic Devices** *IEEE International Electron Devices Meeting (IEDM)*
  Eryilmaz, S. B., Kuzum, D., Jeyasingh, R. G., Kim, S., BrightSky, M., Lam, C., Wong, H. P.
  IEEE.2013
- **Experimental demonstration of a fully digital capacitive sensor interface built entirely using carbon-nanotube FETs**
  Shulaker, M., Rethy, J. V., Hills, G., Chen, H. Y., Gielen, G., Wong, H. S.
  2013
- **Stochastic learning in oxide binary synaptic device for neuromorphic computing** *Frontiers in neuroscience*
  Yu, S., Gao, B., Fang, Z., Yu, H., Kang, J., Wong, H. S.
  2013; 7
- **Sacha: the Stanford carbon nanotube controlled handshaking robot**
  Shulaker, M., Rethy, J. V., Hills, G., Chen, H. Y., Gielen, G., Wong, H. S.
  2013
- **Combinational Logic Design Using Six-Terminal NEM Relays** *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions*
  Lee, D., Lee, W. S., Chen, C., Fallah, F., Provine, J., Chong, S., Wong, H.S.Philip
  2013
- **Effect of Wordline/Bitline Scaling on the Performance, Energy Consumption, and Reliability of Cross-Point Memory Array** *ACM Journal on Emerging Technologies in Computing Systems (JETC)*
  Liang, J., Yeh, S., Wong, S. S., Wong, H. S.
  2013; 1 (9): 9
- **Dilute phosphide nitride materials as photocathodes for electrochemical solar energy conversion** *SPIE OPTO*
  Parameshwaran, V., Xu, X., Kang, Y., Harris, J., Wong, H. S., Clemens, B.
  2013: 86201J-86201J-9
- **Computational simulation of block copolymer directed self-assembly in small topographical guiding templates** *SPIE Advanced Lithography*
  Yi, H., Latypov, A., Wong, H. S.
  2013: 86801L-86801L-7
- **Laterally Actuated Platinum-Coated Polysilicon NEM Relays** *IEEE*
  Parsa, R., Lee, W. S., Shavezipur, M., Provine, J., Maboudian, R., Mitra, S., Wong, H.S.Philip
  2013
- **Compact models of emerging devices** *Electron Devices and Solid-State Circuits (EDSSC), IEEE International*
  Lee, C. S., Yu, S., Guan, X., Luo, J., Wei, L., Wong, H. S.
  2013
- **3D vertical RRAM-Scaling limit analysis and demonstration of 3D array operation**
  Yu, S., Chen, H. Y., Deng, Y., Gao, B., Jiang, Z., Kang, J., Wong, H.S.Philip
  2013

- **Block copolymer directed self-assembly (DSA) aware contact layer optimization for 10 nm 1D standard cell library**
  Du, Y., Guo, D., Wong, M. D., Yi, H., Wong, H. S., Zhang, H.
  2013
- **Technology projections of III–V devices down to 11 nm: importance of electrostatics and series resistance** *Electronics Letters*
  Oh, S., Wong, H. S.
  2013; 13 (49): 832-833
- **Novel graphene-based devices** *Electron Devices and Solid-State Circuits (EDSSC), IEEE International*
  Tian, H., Yang, Y., Xie, D., Chen, H. Y., Wong, H. S., Ren, T. L.
  2013
- **Mass fabrication and delivery of 3D multilayer [mgr] Tags into living cells** *Scientific reports*
  Chen, L. Y., Parizi, K. B., Kosuge, H., Milaninia, K. M., McConnell, M. V., Wong, H. S.
  2013; 3
- **Nanometer-Scale RRAM** *Electron Device Letters, IEEE*
  Zhang, Z., Wu, Y., Wong, H. P., Wong, S. S.
  2013; 8 (34): 1005-1007
- **Carbon nanotube computer** *Nature*
  Shulaker, M. M., Hills, G., Patil, N., Wei, H., Chen, H. Y., Wong, H. S.
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- **(Invited) Carbon 1D/2D Nanoelectronics: Advances in Synthesis and Integration** *ECS Transactions*
  Parker, J. M., Chen, X., Liyanage, L., Tang, A., Wong, H. S.
  2013; 1 (53): 27-38
- **5th International Memory Workshop May 26th–29th 2013 Hyatt Regency Hotel, Monterey, CA**
  Aochi, H., Bernard, D., CEA-Spintec, F., Pei-Ying, D., Hong, K., Asano, I., Wong, H.S.Philip
  2013
- **Compact Model for Carbon Nanotube Field-Effect Transistors Including Nonidealities and Calibrated With Experimental Data Down to 9-nm Gate Length** *IEEE Transactions on Electron Devices*
  Luo, J., Wei, L., Lee, C. S., Franklin, A. D., Wong, H. S.
  2013; 6 (60)
- **A Low Energy Oxide#Based Electronic Synaptic Device for Neuromorphic Visual Systems with Tolerance to Device Variation** *Advanced Materials*
  Yu, S., Gao, B., Fang, Z., Yu, H., Kang, J., Wong, H. S.
  2013
- **Dual-beam, six-terminal nanoelectromechanical relays** *Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS*
  Harrison, K. L., Lee, W. S., Shavezipur, K., Provine, J., Mitra, S., Wong, H. S.
  2013
- **Thermal transport in phase change memory materials** *Annual Review of Heat Transfer*
  Bozorg-Grayeli, E., Reifenberg, J. P., Asheghi, M., Wong, H. S., Goodson, K. E.
  2013; 1 (16)
- **Design strategy of small topographical guiding templates for sub-15nm integrated circuits contact hole patterns using block copolymer directed self assembly** *SPIE Advanced Lithography*
  Yi, H., Bao, X. Y., Tiberio, R., Wong, H. S.
  2013: 868010-868010-9
- **< span> Phase Change Memory–The Interplay Between Thermal and Electrical Effects**
  Wong, H. S.
  2013
- **Carbon nanotube circuits: opportunities and challenges**

Wei, H., Shulaker, M., Hills, G., Chen, H. Y., Lee, C. S., Liyanage, L., Wong, H.S.Philip
2013

- **Phonon and electron transport through Ge 2 Sb 2 Te 5 films and interfaces bounded by metals** *Applied Physics Letters*
  Lee, J., Bozorg-Grayeli, E., Kim, S. B., Asheghi, M., Wong, H. P., Goodson, K. E.
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- **Electrothermal Modeling and Design Strategies for Multibit Phase-Change Memory** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Li, Z., Jeyasingh, R. G., Lee, J., Asheghi, M., Wong, H. P., Goodson, K. E.
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- **Low-Energy Robust Neuromorphic Computation Using Synaptic Devices** *IEEE TRANSACTIONS ON ELECTRON DEVICES*
  Kuzum, D., Jeyasingh, R. G., Yu, S., Wong, H. P.
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- **Increasing the semiconducting fraction in ensembles of single-walled carbon nanotubes** *CARBON*
  Parker, J., Beasley, C., Lin, A., Chen, H., Wong, H. P.
  2012; 50 (14): 5093-5098
- **Graphene Interconnect Lifetime: A Reliability Analysis** *IEEE ELECTRON DEVICE LETTERS*
  Chen, X., Seo, D. H., Seo, S., Chung, H., Wong, H. P.
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- **Optical Absorption Enhancement in Freestanding GaAs Thin Film Nanopyramid Arrays** *ADVANCED ENERGY MATERIALS*
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